MCP37211-200
MCP37D11-200

200 Msps, 12-Bit Low-Power ADC with 8-Channel MUX

Features:

- Sample Rates:
  - 200 Msps for single-channel mode
  - 200 Msps/number of channels used
- SNR with f_{IN} = 15 MHz and -1 dBFS:
  - 71.3 dBFS (typical) for 200 Msps
- SFDR with f_{IN} = 15 MHz and -1 dBFS:
  - 90 dBc (typical) at 200 Msps
- Power Dissipation with LVDS Digital I/O:
  - 468 mW for 200 Msps
- Power Dissipation with CMOS Digital I/O:
  - 436 mW for 200 Msps, Output Clock = 100 MHz
- Power Dissipation Excluding Digital I/O:
  - 387 mW for 200 Msps
- Power Saving Modes:
  - 80 mW during Standby
  - 33 mW during Shutdown
- Supply Voltage:
  - Digital Section: 1.2V, 1.8V
  - Analog Section: 1.2V, 1.8V
- Selectable Input Range: up to 2.975 V_{P-P}
- Input Channel Bandwidth: 500 MHz
- Channel-to-Channel Crosstalk: > 95 dB in Multi-Channel mode (Input = 15 MHz, -1 dBFS)
- Output Data Format:
  - Parallel CMOS, DDR LVDS
- Optional Output Data Randomizer
- Built-In ADC Linearity Calibration Algorithms:
  - Harmonic Distortion Correction (HDC)
  - DAC Noise Cancellation (DNC)
  - Dynamic Element Matching (DEM)
  - Flash Error Calibration
- Digital Signal Post-Processing (DSPP) Options:
  - Decimation Filters
  - Fractional Delay Recovery (FDR) for time-delay corrections in multi-channel operations (dual/octal-channel modes)
  - Noise-Shaping Requantizer (NSR)
  - Phase, Offset and Gain adjust of individual channels
  - Digital Down-Conversion (DDC) with I/Q or f_S/8 output (MCP37D11-200)
  - Continuous Wave Beamforming for octal-channel mode (MCP37D11-200)
- Built-In ADC Linearity Calibration Algorithms:
  - Harmonic Distortion Correction (HDC)
  - DAC Noise Cancellation (DNC)
  - Dynamic Element Matching (DEM)
  - Flash Error Calibration
- Serial Peripheral Interface (SPI)
- Package Options:
  - VTLA-124 (9 mm x 9 mm x 0.9 mm)
  - TFBGA-121 (8 mm x 8 mm x 1.08 mm)
- No external reference decoupling capacitor required for the TFBGA Package
- Industrial Temperature Range: -40°C to +85°C

Typical Applications:

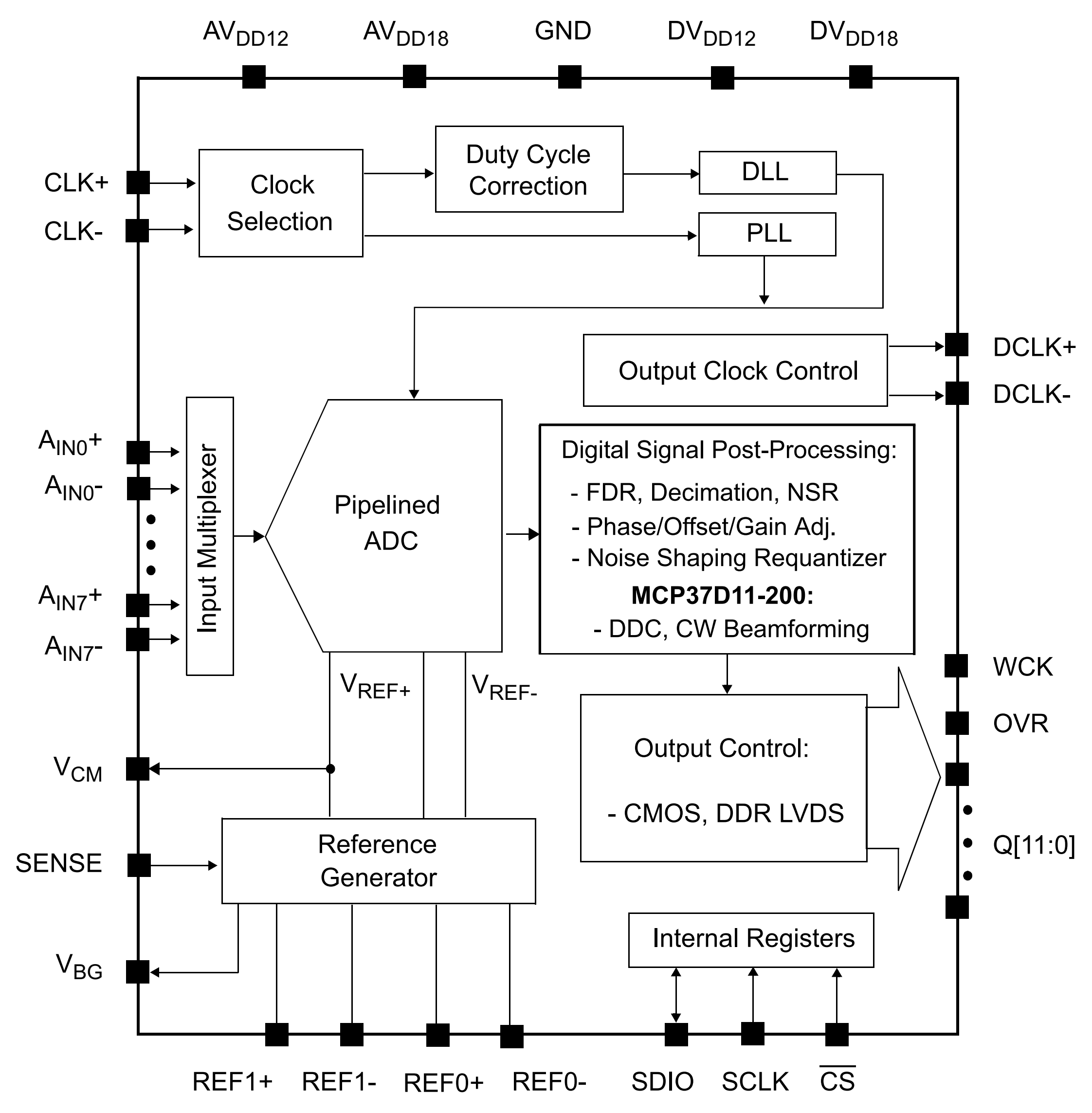
- Communication Instruments
- Cellular Base Stations
- Radar
- Ultrasound and Sonar Imaging
- Scanners and Low-Power Portable Instruments
- Industrial and Consumer Data Acquisition System

MCP372XX/MCP37DXX Family Comparison[1,2]:

Part Number	Sample Rate	Resolution	Digital Decimation[3]	Digital Down-Conversion[4]	CW Beamforming[5]	Noise-Shaping Requantizer[3]
MCP37231-200	200 Msps	16	Yes	No	No	No
MCP37221-200	200 Msps	14	Yes	No	No	No
MCP37211-200	200 Msps	12	Yes	No	No	Yes
MCP37D31-200	200 Msps	16	Yes	Yes	Yes	No
MCP37D21-200	200 Msps	14	Yes	Yes	Yes	No
MCP37D11-200	200 Msps	12	Yes	Yes	Yes	Yes

Note 1: For TFBGA package, contact Microchip Technology Inc. for availability.
2: The devices in the same package type are pin-to-pin compatible.
3: Available in single and dual-channel mode.
4: Available in single and dual-channel mode, and octal-channel mode when CW beamforming is enabled.
5: Available in octal-channel mode.

Functional Block Diagram



General Description:

The MCP37211-200 is Microchip's baseline 12-bit 200 Msps pipelined ADC, featuring built-in high-order digital decimation filters, noise-shaping requantizer, gain and offset adjustment per channel and fractional delay recovery.

The MCP37D11-200 device features digital down-conversion and CW beamforming capability, in addition to the features offered by the MCP37211-200.

All devices feature harmonic distortion correction and DAC noise cancellation, enabling SNR of 71.3 dBFS (typical) and SFDR of 90 dBc (typical).

These A/D converters are exceptionally low power, with only 468 mW power consumption, while using the LVDS interface at 200 Msps.

This superior low-power operation coupled with high dynamic performance make these devices ideal for various high-performance, high-speed data acquisition systems, including communications equipment, radar and portable instrumentation.

In single or dual-channel mode, the Noise-Shaping Requantizer (NSR) feature can allow the ADC to improve SNR beyond a conventional 11 or 12-bit ADC. The NSR reshapes the quantization noise such that most of the noise power is pushed outside the frequency of interest. As a result, SNR is improved significantly within a selected frequency band of interest while SFDR is not affected.

In single or dual-channel mode, the output decimation filter option improves SNR performance up to 73.7 dBFS. The digital down-conversion option in conjunction with the decimation and quadrature output options offer great flexibility in digital communication system design, including cellular base stations and narrow-band communications.

These devices can have up to eight differential input channels through an input MUX. The sampling rate is up to 200 Msps when a single channel is used, or 25 Msps per channel when all 8-input channels are used.

In dual or octal-channel mode, the Fractional Delay Recovery (FDR) feature digitally corrects the difference in sampling instant between different channels, so that all inputs appear to have been sampled at the same time.

The differential full-scale analog input range is programmable up to 2.975 V_{P-P}. The ADC output data can be coded in two's complement or offset binary representation, with or without the data randomizer option. The output data is available as full rate CMOS or double data rate (DDR) LVDS.

The device is available in a Pb-free VTLA-124 and TFBGA-121 packages. The device operates over the commercial temperature range of -40°C to +85°C.

Package Types

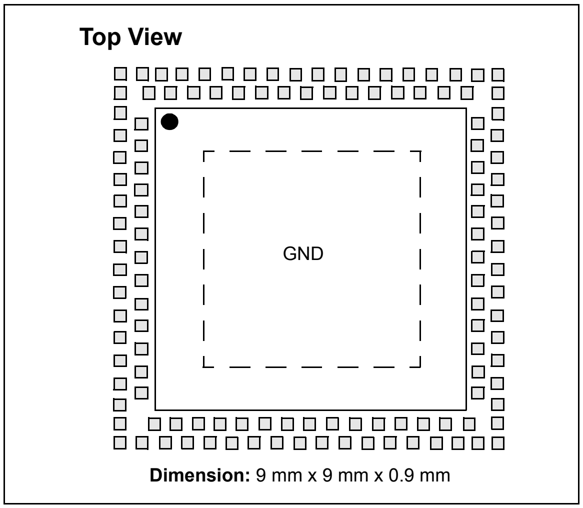


FIGURE 1: VTLA-124 Package.

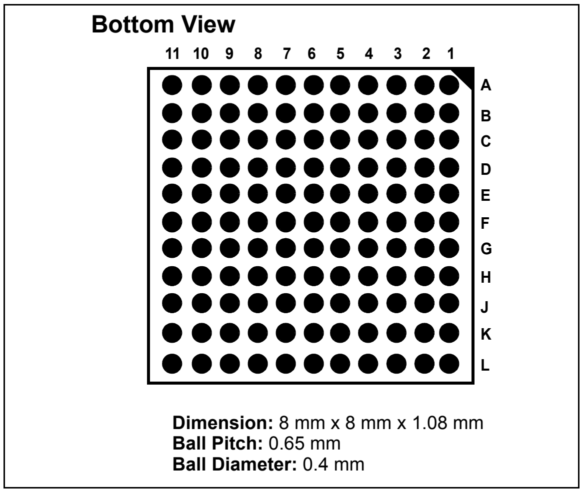
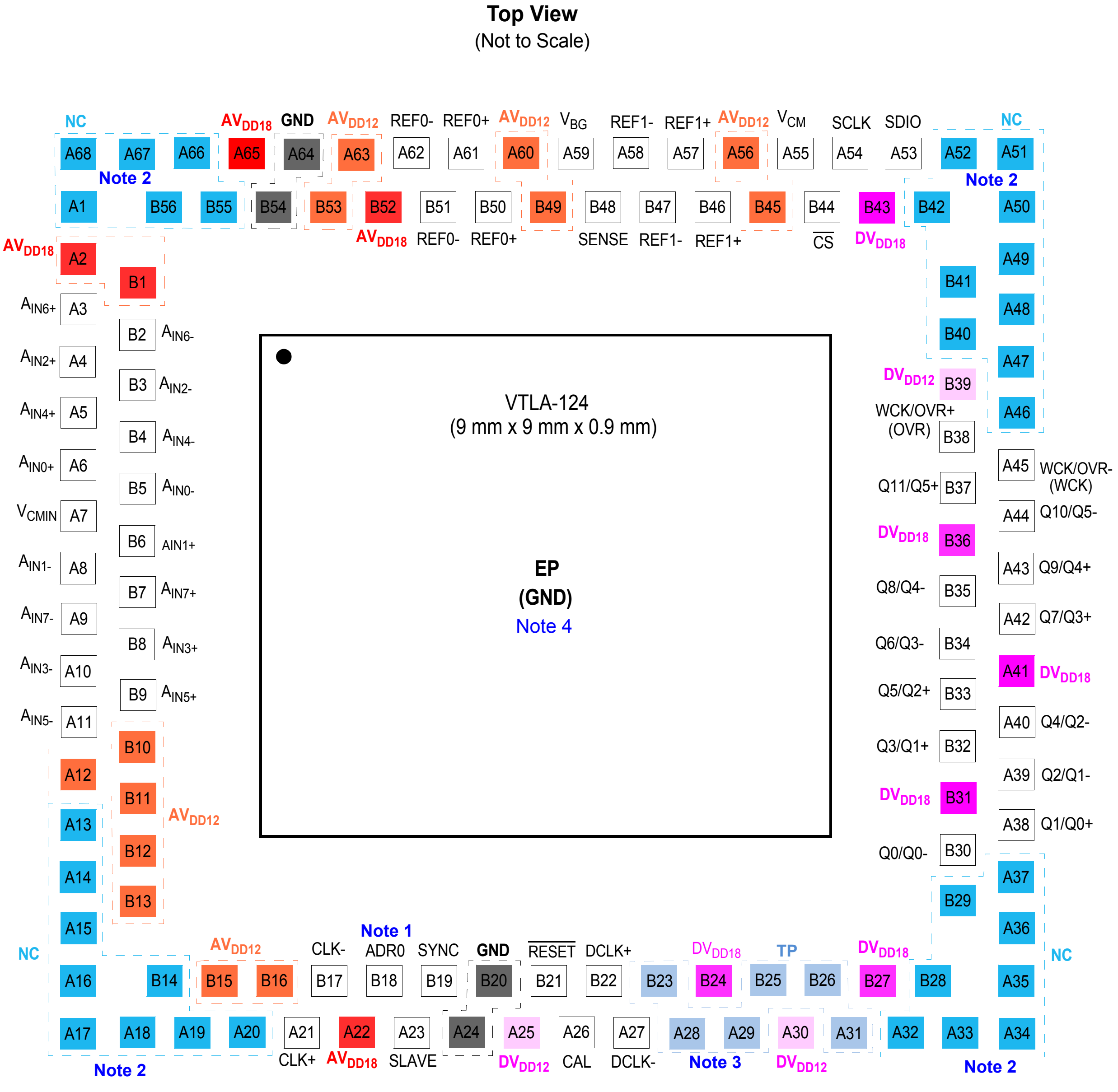


FIGURE 2: TFBGA-121 Package. (Contact Microchip Technology Inc. for availability).

NOTES:

1.0 PACKAGE PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



Note 1: Tie to GND or DV_{DD18}. ADR1 is internally bonded to GND.

2: NC – Not connected pins. These pins can float or be tied to ground.

3: TP – Test pins. Leave these pins floating and do not tie to ground or supply.

4: Exposed pad (EP – back pad of the package) is the common ground (GND) for analog and digital supplies. Connect this pad to a clean ground reference on the PCB.

FIGURE 1-1: *VTLA-124 Package. See Table 1-1 for the pin descriptions.*

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124

Pin No.	Name	I/O Type	Description
Power Supply Pins			
A2, A22, A65, B1, B52	AV_{DD18}	Supply	Supply voltage input (1.8V) for analog section
A12, A56, A60, A63, B10, B11, B12, B13, B15, B16, B45, B49, B53	AV_{DD12}		Supply voltage input (1.2V) for analog section
A25, A30, B39	DV_{DD12}		Supply voltage input (1.2V) for digital section
A41, B24, B27, B31, B36, B43	DV_{DD18}		Supply voltage input (1.8V) for digital section and all digital I/O
EP	GND		Exposed pad: Common ground pin for digital and analog sections
ADC Analog Input Pins			
A3	A_{IN6+}	Analog Input	Channel 6 differential analog input (+)
B2	A_{IN6-}		Channel 6 differential analog input (-)
A4	A_{IN2+}		Channel 2 differential analog input (+)
B3	A_{IN2-}		Channel 2 differential analog input (-)
A5	A_{IN4+}		Channel 4 differential analog input (+)
B4	A_{IN4-}		Channel 4 differential analog input (-)
A6	A_{IN0+}		Channel 0 differential analog input (+)
B5	A_{IN0-}		Channel 0 differential analog input (-)
B6	A_{IN1+}		Channel 1 differential analog input (+)
A8	A_{IN1-}		Channel 1 differential analog input (-)
B7	A_{IN7+}		Channel 7 differential analog input (+)
A9	A_{IN7-}		Channel 7 differential analog input (-)
B8	A_{IN3+}		Channel 3 differential analog input (+)
A10	A_{IN3-}		Channel 3 differential analog input (-)
B9	A_{IN5+}		Channel 5 differential analog input (+)
A11	A_{IN5-}		Channel 5 differential analog input (-)
A21	CLK+		Differential clock input (+)
B17	CLK-		Differential clock input (-)
Reference Pins (Note 1)			
A57, B46	REF1+	Analog Output	Differential reference 1 (+) voltage
A58, B47	REF1-		Differential reference 1 (-) voltage
A61, B50	REF0+		Differential reference 0 (+) voltage
A62, B51	REF0-		Differential reference 0 (-) voltage
SENSE, Bandgap and Common Mode Voltage Pins			
B48	SENSE	Analog Input	Analog input full-scale range selection. See Table 4-2 for SENSE voltage settings.
A59	V_{BG}	Analog Output	Internal bandgap output voltage Connect a decoupling capacitor (2.2 µF)
A7	V_{CMIN}	Analog Input	Common-Mode voltage input for auto-calibration Connect V_{CM} voltage (**Note 2**)
A55	V_{CM}		Common-Mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 µF) (**Note 3**)

TABLE 1-1: PIN FUNCTION TABLE FOR VTLA-124 (CONTINUED)

Pin No.	Name	I/O Type	Description
Digital I/O Pins			
B18	ADR0	Digital Input	SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}. (**Note 4**)
A23	SLAVE		Not used. Tie to GND.
B19	SYNC	Digital Input/ Output	Not used. Leave this pin floating.
B21	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High:** Normal operating mode **Low:** Reset mode (**Note 5**)
A26	CAL	Digital Output	Calibration status flag digital output: **High:** Calibration is complete **Low:** Calibration is not complete (**Note 5**)
B22	DCLK+		**LVDS**: Differential digital clock output (+) **CMOS:** Digital clock output (**Note 7**)
A27	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)
ADC Output Pins (Note 8)			
B30	Q0/Q0-	Digital Output	Digital data output: CMOS = Q0, DDR LVDS = Q0-
A38	Q1/Q0+		Digital data output: CMOS = Q1, DDR LVDS = Q0+
A39	Q2/Q1-		Digital data output: CMOS = Q2, DDR LVDS = Q1-
B32	Q3/Q1+		Digital data output: CMOS = Q3, DDR LVDS = Q1+
A40	Q4/Q2-		Digital data output: CMOS = Q4, DDR LVDS = Q2-
B33	Q5/Q2+		Digital data output: CMOS = Q5, DDR LVDS = Q2+
B34	Q6/Q3-		Digital data output: CMOS = Q6, DDR LVDS = Q3-
A42	Q7/Q3+		Digital data output: CMOS = Q7, DDR LVDS = Q3+
B35	Q8/Q4-		Digital data output: CMOS = Q8, DDR LVDS = Q4-
A43	Q9/Q4+		Digital data output: CMOS = Q9, DDR LVDS = Q4+
A44	Q10/Q5-		Digital data output: CMOS = Q10, DDR LVDS = Q5-
B37	Q11/Q5+		Digital data output: CMOS = Q11, DDR LVDS = Q5+
B38	WCK/OVR+ (OVR)		**WCK:** Word clock sync digital output **OVR:** Input over-range indication digital output (**Note 9**)
A45	WCK/OVR- (WCK)		
SPI Interface Pins			
A53	SDIO	Digital Input/Output	SPI data input/output
A54	SCLK	Digital Input	SPI serial clock input
B44	$\overline{\text{CS}}$		SPI Chip Select input
Not Connected Pins			
A1, A13 - A20, A32 - A37, A46 - A52, A66 - A68, B14, B28, B29, B40, B41, B42, B55, B56	NC		These pins can be tied to ground or left floating.
Pins that need to be grounded			
A24, A64, B20, B54	GND		These pins are not supply pins, but need to be tied to ground.
Output Test Pins			
A28, A29, A31, B23, B25, B26	TP	Digital Output	Output test pins. Do not use. Always Leave these pins floating. (**Note 10**)

Notes:

1. These pins are internal reference voltage outputs. They should not be driven. External decoupling circuits are required. See **Section 4.5.3 "SNR/SFDR Performance vs. SENSE Selection"** for details.
2. V_{CMIN} is used for Auto-Calibration only. $V_{CMIN}+$ and $V_{CMIN}-$ should always be tied together. There should be no voltage difference between the two pins. Typically, both $V_{CMIN}+$ and $V_{CMIN}-$ are tied to the V_{CM} output pin, but they can be tied to another common mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
3. When the V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor and should be directly tied to $V_{CMIN}+$ and $V_{CMIN}-$ pins.
4. ADR1 (for A1 bit) is internally bonded to GND (`'0'`). If ADR0 is dynamically controlled, ADR0 must be held constant while $\overline{\text{CS}}$ is "Low".
5. The device is in Reset mode while this pin stays "Low". On the rising edge of $\overline{\text{RESET}}$, the device exits the Reset mode, initializes all internal user registers to default values and begins power-up calibration.
6. The CAL pin stays "Low" at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has "High" output. It stays "High" until the internal calibration is restarted by hardware or Soft Reset command. In Reset mode, this pin is "Low". In Standby and Shutdown modes, this pin will maintain the prior condition.
7. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the DSPP, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
8. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The even data bits (Q0, Q2, Q4, Q6, Q8, Q10) appear when DCLK+ is "High". The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11) appear when DCLK+ is "Low". See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figure 2-2 for LVDS output timing diagram.
9. **CMOS output mode:** WCK/OVR+ is OVR and WCK/OVR- is WCK.
   DDR LVDS output mode: The rising edge of DCLK+ is OVR and the falling edge is WCK.
   OVR: OVR will be held "High" when analog input over-range is detected. Digital post-processing will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: Normally "Low". "High" while data from the first channel is sent out.
10. Do not tie to ground or supply.

Top View
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11
A	SDIO	V_{CM}	REF1+	REF1-	V_{BG}	REF0+	REF0-	GND	GND	A_{IN4-}	A_{IN2+}
B	SCLK	$\overline{CS}$	GND	GND	SENSE	AV_{DD12}	AV_{DD12}	AV_{DD18}	AV_{DD18}	A_{IN4+}	A_{IN2-}
C	WCK/ OVR- (WCK)	WCK/ OVR+ (OVR)	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN6-}	A_{IN0+}
D	Q10/Q5-	Q11/Q5+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN6+}	A_{IN0-}
E	Q8/Q4-	Q9/Q4+	GND	GND	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN5+}	A_{IN1+}
F	Q6/Q3-	Q7/Q3+	DV_{DD18}	DV_{DD18}	AV_{DD12}	AV_{DD12}	AV_{DD12}	GND	GND	A_{IN5-}	A_{IN1-}
G	Q4/Q2-	Q5/Q2+	DV_{DD18}	DV_{DD18}	GND	GND	AV_{DD12}	AV_{DD12}	GND	A_{IN7-}	A_{IN3+}
H	Q2/Q1-	Q3/Q1+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	A_{IN7+}	A_{IN3-}
J	Q0/Q0-	Q1/Q0+	DV_{DD12}	DV_{DD12}	GND	GND	GND	GND	GND	V_{CMIN}+	V_{CMIN}-
K	TP	TP	TP	DCLK-	CAL	GND	SLAVE	ADR0	ADR1	GND	GND
L	TP	TP	TP	DCLK+	$\overline{RESET}$	SYNC	GND	CLK+	CLK-	GND	AV_{DD18}

🟩 Analog
🟨 Digital
All others: Supply Voltage

Note 1: Die dimension: 8 mm x 8 mm x 1.08 mm.
2: Ball dimension: (a) Ball Pitch = 0.65 mm, (b) Ball Diameter = 0.4 mm.
3: Flip-chip solder ball composition: Sn with Ag 1.8%.
4: Solder sphere composition: SAC-405 (Sn/Au 4%/Cu 0.5%).

FIGURE 1-2: *TFBGA-121 Package. See Table 1-2 for the pin descriptions. Decoupling capacitors for reference pins and V_{BG} are embedded in the package. Leave TP pins floating always.*

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121

Ball No.	Name	I/O Type	Description
A1	SDIO	Digital Input/Output	SPI data input/output
A2	V_{CM}	Analog Output	Common-Mode output voltage (900 mV) for analog input signal Connect a decoupling capacitor (0.1 µF) (**Note 1**)
A3	REF1+		Differential reference voltage 1 (+/-). Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A4	REF1-		
A5	V_{BG}		Internal bandgap output voltage A decoupling capacitor (2.2 µF) is embedded in the TFBGA package. Leave this pin floating.
A6	REF0+		Differential reference 0 (+/-) voltage. Decoupling capacitors are embedded in the TFBGA package. Leave these pins floating.
A7	REF0-		
A8, A9	GND	Supply	Common ground for analog and digital sections
A10	A_{IN4-}	Analog Input	Channel 4 differential analog input (-)
A11	A_{IN2+}		Channel 2 differential analog input (+)
B1	SCLK	Digital Input	SPI serial clock input
B2	$\overline{CS}$		SPI Chip Select input
B3, B4	GND	Supply	Common ground for analog and digital sections
B5	SENSE	Analog Input	Analog input range selection. See Table 4-2 for SENSE voltage settings.
B6, B7	AV_{DD12}	Supply	Supply voltage input (1.2V) for analog section
B8, B9	AV_{DD18}		Supply voltage input (1.8V) for analog section
B10	A_{IN4+}	Analog Input	Channel 4 differential analog input (+)
B11	A_{IN2-}		Channel 2 differential analog input (-)
C1	WCK/OVR- (WCK)	Digital Output	**WCK:** Word clock sync digital output **OVR:** Input over-range indication digital output (**Note 2**)
C2	WCK/OVR+ (OVR)		
C3, C4	GND	Supply	Common ground for analog and digital sections
C5 - C7	AV_{DD12}		Supply voltage input (1.2V) for analog section
C8, C9	GND		Common ground pin for analog and digital sections
C10	A_{IN6-}	Analog Input	Channel 6 differential analog input (-)
C11	A_{IN0+}		Channel 0 differential analog input (+)
D1	Q10/Q5-	Digital Output	Digital data output: (**Note 3**) CMOS = Q10, DDR LVDS = Q5-
D2	Q11/Q5+		Digital data output: (**Note 3**) CMOS = Q11, DDR LVDS = Q5+
D3, D4	GND	Supply	Common ground for analog and digital sections
D5 - D7	AV_{DD12}		Supply voltage input (1.2V) for analog section
D8, D9	GND		Common ground for analog and digital sections
D10	A_{IN6+}	Analog Input	Channel 6 differential analog input (+)
D11	A_{IN0-}		Channel 0 differential analog input (-)
E1	Q8/Q4-	Digital Output	Digital data output: (**Note 3**) CMOS = Q8, DDR LVDS = Q4-
E2	Q9/Q4+		Digital data output: (**Note 3**) CMOS = Q9, DDR LVDS = Q4+
E3, E4	GND	Supply	Common ground for analog and digital sections
E5 - E7	AV_{DD12}		Supply voltage input (1.2V) for analog section
E8, E9	GND		Common ground for analog and digital sections
E10	A_{IN5+}	Analog Input	Channel 5 differential analog input (+)
E11	A_{IN1+}		Channel 1 differential analog input (+)

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
F1	Q6/Q3-	Digital Output	Digital data output: **(Note 3)** CMOS = Q6, DDR LVDS = Q3-
F2	Q7/Q3+		Digital data output: **(Note 3)** CMOS = Q7, DDR LVDS = Q3+
F3	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential.
F4			
F5 - F7	AV_{DD12}		Supply voltage input (1.2V) for analog section
F8, F9	GND		Common ground for analog and digital sections
F10	A_{IN5-}	Analog Input	Channel 5 differential analog input (-)
F11	A_{IN1-}		Channel 1 differential analog input (-)
G1	Q4/Q2-	Digital Output	Digital data output: **(Note 3)** CMOS = Q4, DDR LVDS = Q2-
G2	Q5/Q2+		Digital data output: **(Note 3)** CMOS = Q5, DDR LVDS = Q2+
G3, G4	DV_{DD18}	Supply	Supply voltage input (1.8V) for digital section. All digital input pins are driven by the same DV_{DD18} potential.
G5, G6	GND		Common ground for analog and digital sections
G7, G8	AV_{DD12}		Supply voltage input (1.2V) for analog section
G9	GND		Common ground for analog and digital sections
G10	A_{IN7-}	Analog Input	Channel 7 differential analog input (-)
G11	A_{IN3+}		Channel 3 differential analog input (+)
H1	Q2/Q1-	Digital Output	Digital data output: **(Note 3)** CMOS = Q2, DDR LVDS = Q1-
H2	Q3/Q1+		Digital data output: **(Note 3)** CMOS = Q3, DDR LVDS = Q1+
H3, H4	DV_{DD12}	Supply	Supply voltage input (1.2V) for digital section
H5 - H9	GND		Common ground for analog and digital sections
H10	A_{IN7+}	Analog Input	Channel 7 differential analog input (+)
H11	A_{IN3-}		Channel 3 differential analog input (-)
J1	Q0/Q0-	Digital Output	Digital data output: **(Note 3)** CMOS = Q0, DDR LVDS = Q0-
J2	Q1/Q0+		Digital data output: **(Note 3)** CMOS = Q1, DDR LVDS = Q0+
J3, J4	DV_{DD12}	Supply	DC supply voltage input pin for digital section (1.2V)
J5 - J9	GND		Common ground for analog and digital sections
J10	V_{CMIN+}	Analog Input	Common-Mode voltage input for auto-calibration **(Note 4)** These two pins should be tied together and connected to V_{CM} voltage.
J11	V_{CMIN-}		
K1 - K3	TP	Digital Output	Output test pins. Leave these pins floating always. **(Note 9)**
K4	DCLK-		**LVDS:** Differential digital clock output (-) **CMOS:** Unused (leave floating)
K5	CAL		Calibration status flag digital output **(Note 5):** **High:** Calibration is complete **Low:** Calibration is not complete
K6	GND	Supply	Common ground pin for analog and digital sections
K7	SLAVE	Digital Input	Not used. Tie this pin to GND.
K8	ADR0		SPI address selection pin (A0 bit). Tie to GND or DV_{DD18}. **(Note 6)**
K9	ADR1		SPI address selection pin (A1 bit). Tie to GND or DV_{DD18}. **(Note 6)**
K10, K11	GND	Supply	Common ground for analog and digital sections
L1 - L3	TP	Digital Output	Output test pins. Leave these pins floating always. **(Note 9)**

TABLE 1-2: PIN FUNCTION TABLE FOR TFBGA-121 (CONTINUED)

Ball No.	Name	I/O Type	Description
L4	DCLK+	Digital Output	**LVDS:** Differential digital clock output (+) **CMOS:** Digital clock output (**Note 7**)
L5	$\overline{\text{RESET}}$	Digital Input	Reset control input: **High**: Normal operating mode **Low:** Reset mode (**Note 8**)
L6	SYNC	Digital Input/Output	Not used. Leave this pin floating
L7	GND	Supply	Common ground for analog and digital sections
L8	CLK+	Analog Input	Differential clock input (+)
L9	CLK-		Differential clock input (-)
L10	GND	Supply	Common ground for analog and digital sections
L11	AV_{DD18}	Analog Input	Supply voltage input (1.8V) for analog section

Notes:

1. When V_{CM} output is used for the common-mode voltage of analog inputs (i.e. by connecting to the center-tap of a balun), the V_{CM} pin should be decoupled with a 0.1 µF capacitor and should be directly tied to the V_{CMIN}+ and V_{CMIN}- pins.
2. **CMOS output mode:** WCK/OVR- is WCK and WCK/OVR+ is OVR.
   DDR LVDS output mode: The rising edge of DCLK+ is OVR and the falling edge is WCK.
   OVR: OVR will be held “High” when analog input over-range is detected. Digital post-processing will cause OVR to assert early relative to the output data. See Figure 2-2 for LVDS timing of these bits.
   WCK: Normally “Low”. “High” while data from the first channel is sent out.
3. **DDR LVDS:** Two data bits are multiplexed onto each differential output pair. The even data bits (Q0, Q2, Q4, Q6, Q8, Q10) appear when DCLK+ is “High”. The odd data bits (Q1, Q3, Q5, Q7, Q9, Q11) appear when DCLK+ is “Low”. See Addresses 0x65 (Register 5-23) and 0x68 (Register 5-26) for output polarity control. See Figure 2-2 for LVDS output timing diagram.
4. V_{CMIN} is used for Auto-Calibration only. V_{CMIN}+ and V_{CMIN}- should always be tied together. There should be no voltage difference between the two pins. Typically, both V_{CMIN}+ and V_{CMIN}- are tied to the V_{CM} output pin, but they can be tied to another common mode voltage if external V_{CM} is used. This pin has High Z input in Shutdown, Standby and Reset modes.
5. The CAL pin stays “Low” at power-up until the first power-up calibration is completed. When the first calibration has completed, this pin has “High” output. It stays “High” until the internal calibration is restarted by hardware or Soft Reset command. In Reset mode, this pin is “Low”. In Standby and Shutdown modes, this pin will maintain the prior condition.
6. If the SPI address is dynamically controlled, the Address pins must be held constant while $\overline{\text{CS}}$ is “Low”.
7. The phase of DCLK relative to the data output bits may be adjusted depending on the operating mode. This is controlled differently depending on the configuration of the digital post-processing, PLL and/or DLL. See also Addresses 0x52, 0x64 and 0x6D (Registers 5-7, 5-22 and 5-28) for more details.
8. The device is in Reset mode while this pin stays “Low”. On the rising edge of $\overline{\text{RESET}}$, the device exits the Reset mode, initializes all internal user registers to default values and begins power-up calibration.
9. Do not tie to ground or supply.

2.0 ELECTRICAL SPECIFICATIONS

2.1 Absolute Maximum Ratings†

Analog and Digital Supply Voltage (AV_{DD12}, DV_{DD12}) .... -0.3V to 1.32V

Analog and Digital Supply Voltage (AV_{DD18}, DV_{DD18}) .... -0.3V to 1.98V

All inputs and outputs w.r.t GND ....–0.3V to AV_{DD18} + 0.3V

Differential Input Voltage .... |AV_{DD18} – GND|

Current at Input Pins ....±2 mA

Current at Output and Supply Pins ....±250 mA

Storage Temperature ....-65°C to +150°C

Ambient Temp. with power applied (T_A)........-55°C to +125°C

Maximum Junction Temperature (T_J).......................... +150°C

ESD protection on all pins......................................2 kV HBM

Solder Reflow Profile .... See Microchip Application Note AN233

Notice†: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Electrical Specifications

TABLE 2-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Requirements						
Analog Supply Voltage	AV_{DD18}	1.71	1.8	1.89	V	
	AV_{DD12}	1.14	1.2	1.26	V	
Digital Supply Voltage	DV_{DD18}	1.71	1.8	1.89	V	**Note 1**
	DV_{DD12}	1.14	1.2	1.26	V	
Analog Supply Current						
Analog Supply Current during Conversion	I_{DD_A18}	—	27	46	mA	at AV_{DD18} Pin
	I_{DD_A12}	—	185	252	mA	at AV_{DD12} Pin
Digital Supply Current						
Digital Supply Current during Conversion	I_{DD_D12}	—	97	226	mA	at DV_{DD12} Pin
Digital I/O Current in CMOS Output Mode	I_{DD_D18}	—	27	—	mA	at DV_{DD18} Pin DCLK = 100 MHz
Digital I/O Current in LVDS Mode	I_{DD_D18}	Measured at DV_{DD18} Pin				
		—	45	66	mA	3.5 mA mode
			33	—	mA	1.8 mA mode
			57			5.4 mA mode
Supply Current during Power Saving Modes						
During Standby Mode	$I_{STANDBY\_AN}$	—	21	—	mA	Address 0x00<4:3> = `1,1` (**Note 2**)
	$I_{STANDBY\_DIG}$	—	41	—		
During Shutdown Mode	I_{DD_SHDN}	—	25	—	mA	Address 0x00<7,0> = `1,1` (**Note 3**)

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
PLL Circuit						
PLL Circuit Current	I_{DD_PLL}	—	21	—	mA	PLL enabled. Included in analog supply current specification.
Total Power Dissipation (Note 4)						
Power Dissipation during conversion, excluding digital I/O	P_{DISS_ADC}	—	387	—	mW	
Total Power Dissipation during conversion with CMOS output mode	P_{DISS_CMOS}	—	436	—	mW	f_S = 200 Msps, DCLK = 100 MHz
Total Power Dissipation during conversion with LVDS output mode	P_{DISS_LVDS}	—	468	—	mW	3.5 mA mode
			446	—		1.8 mA mode
			490			5.4 mA mode
During Standby Mode	$P_{DISS\_STANDBY}$	—	80.4	—	mW	Address 0x00<4:3> = `1,1` (Note 2)
During Shutdown Mode	P_{DISS_SHDN}	—	33	—	mW	Address 0x00<7,0> = `1,1` (Note 3)
Power-On Reset (POR) Voltage						
Threshold Voltage	V_{POR}	—	800	—	mV	Applicable to AV_{DD12} only
Hysteresis	V_{POR_HYST}	—	40	—	mV	(POR tracks AV_{DD12})
SENSE Input (Note 5, Note 7)						
SENSE Input Voltage	V_{SENSE}	GND	—	AV_{DD12}	V	V_{SENSE} selects reference
SENSE Pin Input Resistance	R_{IN_SENSE}	—	500	—	Ω	To virtual ground at 0.55V. 400 mV < V_{SENSE} < 800 mV
Current Sink into SENSE Pin	I_{SENSE}	—	500	—	µA	SENSE = 0.8V
Reference and Common Mode Voltages						
Internal Reference Voltage (Selected by V_{SENSE})	V_{REF}	—	0.74	—	V	V_{SENSE} = GND
		—	1.49	—		V_{SENSE} = AV_{DD12}
		—	1.86 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV
Common Mode Voltage Output	V_{CM}	—	0.9	—	V	Available at V_{CM} pin
Reference Voltage Output (Note 7, Note 8)	V_{REF1}	—	0.4	—	V	V_{SENSE} = GND
		—	0.8	—		V_{SENSE} = AV_{DD12}
		—	0.4 – 0.8	—		400 mV < V_{SENSE} < 800 mV
	V_{REF0}	—	0.7	—	V	V_{SENSE} = GND
		—	1.4	—		V_{SENSE} = AV_{DD12}
		—	0.7 – 1.4	—		400 mV < V_{SENSE} < 800 mV
Bandgap Voltage Output	V_{BG}	—	0.55	—	V	Available at V_{BG} pin
Analog Inputs						
Full Scale Differential Analog Input Range (Note 5, Note 7)	A_{FS}	—	1.4875	—	V_{P-P}	V_{SENSE} = GND
		—	2.975	—		V_{SENSE} = AV_{DD12}
		—	3.71875 x V_{SENSE}	—		400 mV < V_{SENSE} < 800 mV

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Analog Input 3 dB Bandwidth	f_{IN_3dB}	—	500	—	MHz	With 50Ω source
Differential Input Capacitance	C_{IN}	5	6	7	pF	**Note 5**, **Note 9**
Analog Input Channel Crosstalk	X_{TALK}	—	100	—	dBc	A_{IN}=-1 dBFS at 12 MHz **Note 10**
Analog Input Leakage Current (A_{IN}+, A_{IN}- pins)	I_{LI_AH}	—	—	+1	µA	V_{IH} = AV_{DD12}
	I_{LI_AL}	-1	—	—	µA	V_{IL} = GND
ADC Conversion Rate (Note 11)						
Conversion Rate	f_S	40	—	200	Msps	Tested at 200 Msps
Clock Inputs (CLK+, CLK-) (Note 12)						
Clock Input Frequency	f_{CLK}	—	—	250	MHz	**Note 5**
Differential Input Voltage	V_{CLK_IN}	300	—	800	mV_{P-P}	**Note 5**
Clock Jitter	CLK_{JITTER}	—	175	—	f_{SRMS}	**Note 5**
Clock Input Duty Cycle (**Note 5**)		49	50	51	%	Duty cycle correction disabled
		30	50	70	%	Duty cycle correction enabled
Input Leakage Current at CLK input pin	I_{LI_CLKH}	—	—	+110	µA	V_{IH} = AV_{DD12}
	I_{LI_CLKL}	-10	—	—	µA	V_{IL} = GND
Converter Accuracy (Note 6)						
ADC Resolution (with no missing code)		—	—	12	bits	
Offset Error		—	±0.31	±3.8	LSB	
Gain Error	G_{ER}	—	±0.5	—	% of FS	
Integral Nonlinearity	INL	—	±0.125	—	LSB	
Differential Nonlinearity	DNL	—	±0.03	—	LSB	
Analog Input Common-Mode Rejection Ratio	$CMRR_{DC}$	—	70	—	dB	DC measurement
DC Power Supply Rejection Ratio (PSRR)	$PSRR_{DC}$	—	-117	—	dB	DC measurement
Dynamic Accuracy (Note 6)						
Spurious-Free Dynamic Range	SFDR	78	90	—	dBc	f_{IN} = 15 MHz
		77	85	—	dBc	f_{IN} = 70 MHz
Signal-to-Noise Ratio	SNR	70.63	71.33	—	dBFS	f_{IN} = 15 MHz
	SNR	—	71.09	—	dBFS	f_{IN} = 70 MHz
Effective Number of Bits (ENOB) (**Note 13**)	ENOB	11.44	11.56	—	bits	f_{IN} = 15 MHz
	ENOB	—	11.52	—	bits	f_{IN} = 70 MHz
Total Harmonic Distortion (first 13 harmonics)	THD	78	89	—	dBc	f_{IN} = 15 MHz
		77	82	—	dBc	f_{IN} = 70 MHz
Worst Second or Third Harmonic Distortion	HD2 or HD3	—	90	—	dBc	f_{IN} = 15 MHz
		—	83	—	dBc	f_{IN} = 70 MHz

TABLE 2-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Two-Tone Intermodulation Distortion f_{IN1} = 17.6 MHz, f_{IN2} = 20.6 MHz	IMD	—	90.5	—	dBc	A_{IN} = -7 dBFS, with two input frequencies
Digital Logic Input and Output (Except LVDS Output)						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7 DV_{DD18}	—	DV_{DD18}	V	
Schmidt Trigger Low-Level Input Voltage	V_{IL}	GND	—	0.3 DV_{DD18}	V	
Hysteresis of Schmitt Trigger Inputs (All digital inputs)	V_{HYST}	—	0.05 DV_{DD18}	—	V	
Low-Level Output Voltage	V_{OL}	—	—	0.3	V	I_{OL} = -3 mA, all digital I/O pins
High-Level Output Voltage	V_{OH}	DV_{DD18} – 0.5	1.8	—	V	I_{OL} = + 3mA, all digital I/O pins
Digital Data Output (CMOS Mode)						
Maximum External Load Capacitance	C_{LOAD}	—	10	—	pF	From output pin to GND
Internal I/O Capacitance	C_{INT}	—	4	—	pF	**Note 5**
Digital Data Output (LVDS Mode) (Note 5)						
LVDS High-Level Differential Output Voltage	V_{H_LVDS}	200	300	400	mV	100 Ω differential termination, LVDS bias = 3.5 mA
LVDS Low-Level Differential Output Voltage	V_{L_LVDS}	-400	-300	-200	mV	100 Ω differential termination, LVDS bias = 3.5 mA
LVDS Common Mode Voltage	V_{CM_LVDS}	1	1.15	1.4	V	
Output Capacitance	C_{INT_LVDS}	—	4	—	pF	Internal capacitance from output pin to GND
Differential Load Resistance (LVDS)	R_{LVDS}	—	100	—	Ω	Across LVDS output pairs
Input Leakage Current on Digital I/O Pins						
Data Output Pins	I_{LI_DH}	—	—	+1	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-1	—	—	µA	V_{IL} = GND
I/O Pins except Data Output Pins	I_{LI_DH}	—	—	+6	µA	V_{IH} = DV_{DD18}
	I_{LI_DL}	-35	—	—	µA	V_{IL} = GND (**Note 14**)

Notes:

1. This 1.8V digital supply voltage is used for the digital I/O circuit, including SPI, CMOS and LVDS data output drivers.
2. Standby mode: Most of the internal circuits are turned off, except for internal reference, clock, bias circuits and SPI interface.
3. Shutdown mode: All circuits including reference and clock are turned off, except for the SPI interface.
4. The total power dissipation (typical) is calculated by using the following equation: P_{DISS} = 1.8V x (I_{DD_A18} + I_{DD_D18}) + 1.2V x (I_{DD_A12} + I_{DD_D12}), where I_{DD_D18} is the digital I/O current for LVDS or CMOS output.
5. This parameter is ensured by design and not 100% tested.
6. This parameter is ensured by characterization and not 100% tested.
7. See Table 4-2 for details.
8. Differential reference voltage output at REF1+/- and REF0+/- pins. $V_{REF1} = V_{REF1}+ - V_{REF1}-$. $V_{REF0} = V_{REF0}+ - V_{REF0}-$. These references should not be driven.
9. Input capacitance refers to the effective capacitance between one differential input pin pair.
10. Channel Crosstalk is measured when A_{IN} = -1 dBFS at 12 MHz is applied on one channel while other channel(s) are terminated with 50Ω. See Figure 3-45 for details.
11. ADC core conversion rate. In multi-channel mode, the conversion rate of an individual channel is f_S/N, where N is the number of input channels used.
12. See Figure 4-8 for details on the clock input circuit.
13. ENOB = (SINAD – 1.76)/6.02.
14. This leakage current is due to the internal pull-up resistor.

TABLE 2-2: TIMING REQUIREMENTS – LVDS AND CMOS OUTPUTS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Aperture Delay	t_A	—	1	—	ns	Note 1
Out-of-Range Recovery Time	t_{OVR}	—	1	—	Clocks	Note 1
Output Clock Duty Cycle		—	50	—	%	Note 1
Pipeline Latency	$T_{LATENCY}$	—	28	—	Clocks	Note 2, Note 4
System Calibration (Note 1)						
Power-Up Calibration Time	T_{PCAL}	—	2^{27}	—	Clocks	First 2^{27} sample clocks after power-up
Background Calibration Update Rate	T_{BCAL}	—	2^{30}	—	Clocks	Per 2^{30} sample clocks after T_{PCAL}
$\overline{\text{RESET}}$ Low Time	T_{RESET}	5	—	—	ns	See Figure 2-6 for details. (Note 1)
LVDS Data Output Mode						
Input Clock to Output Clock Propagation Delay	t_{CPD}	—	—	3.2	ns	
Output Clock to Data Propagation Delay	t_{DC}	-0.25	—	+0.25	ns	Note 1
Input Clock to Output Data Propagation Delay	t_{PD}	—	—	3.25	ns	
Rise Time (20% to 80% of output amplitude) (Note 2, Note 3)	t_{RISE_DATA}	—	0.25	0.5	ns	
	t_{RISE_CLK}	—	0.25	0.5	ns	
Fall Time (80% to 20% of output amplitude) (Note 2, Note 3)	t_{FALL_DATA}	—	0.25	0.5	ns	
	t_{FALL_CLK}	—	0.25	0.5	ns	
CMOS Data Output Mode						
Input Clock to Output Clock Propagation Delay	t_{CPD}	TBD			ns	DCLK = 100 MHz
Output Clock to Data Propagation Delay	t_{DC}	TBD			ns	DCLK = 100 MHz
Input Clock to Output Data Propagation Delay	t_{PD}	TBD			ns	DCLK = 100 MHz
Rise Time (20% to 80% of output amplitude)	t_{RISE_DATA}	TBD			ns	DCLK = 100 MHz
	t_{RISE_CLK}	TBD			ns	DCLK = 100 MHz
Fall Time (80% to 20% of output amplitude)	t_{FALL_DATA}	TBD			ns	DCLK = 100 MHz
	t_{FALL_CLK}	TBD			ns	DCLK = 100 MHz

Note 1: This parameter is ensured by design, but not tested 100% in production.

2: This parameter is ensured by characterization, but not tested 100% in production.

3: t_{RISE} = approximately less than 10% of duty cycle.

4: Output latency is measured without using decimation filter and digital down-converter options.

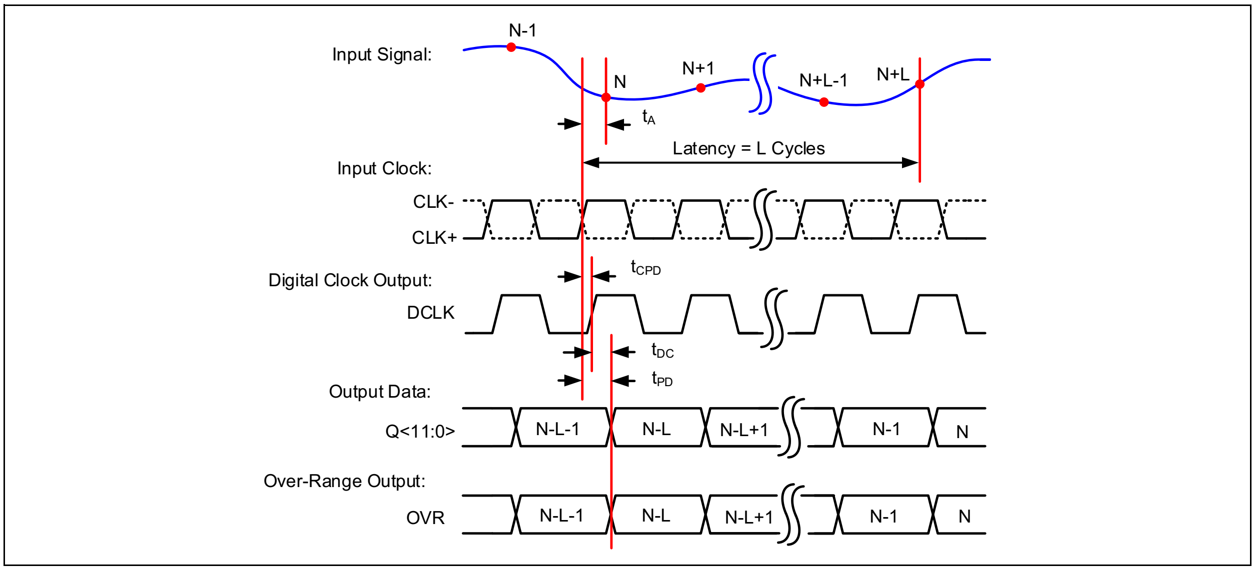


FIGURE 2-1: *Timing Diagram – CMOS Output.*

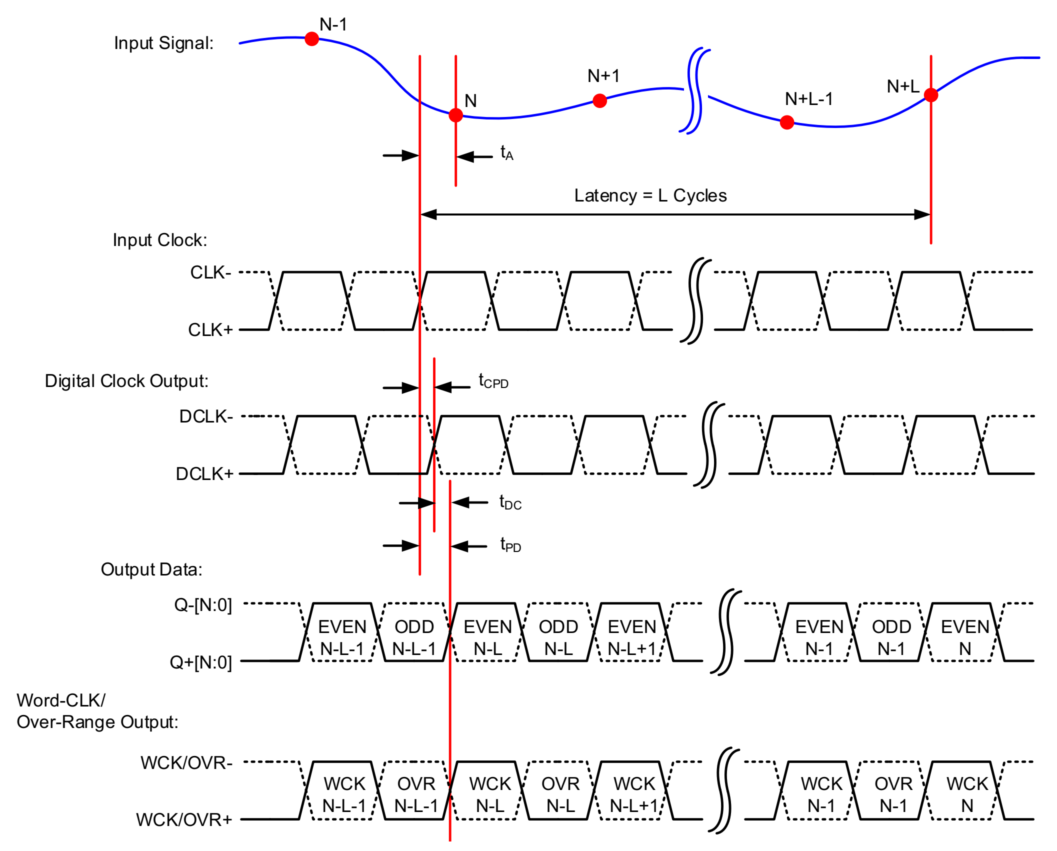


FIGURE 2-2: *Timing Diagram – LVDS Output with Even Bit First.*

TABLE 2-3: SPI SERIAL INTERFACE TIMING SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, $AV_{DD18} = DV_{DD18}$ = 1.8V, $AV_{DD12} = DV_{DD12}$ = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value. All timings are measured at 50%.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Serial Clock frequency, f_{SCK} = 50 MHz						
$\overline{CS}$ setup time	t_{CSS}	10	—	—	ns	
$\overline{CS}$ hold time	t_{CSH}	20	—	—	ns	
$\overline{CS}$ disable time	t_{CSD}	20	—	—	ns	
Data setup time	t_{SU}	2	—	—	ns	
Data hold time	t_{HD}	4	—	—	ns	
Serial Clock high time	t_{HI}	8	—	—	ns	
Serial Clock low time	t_{LO}	8	—	—	ns	**Note 1**
Serial Clock delay time	t_{CLD}	20	—	—	ns	
Serial Clock enable time	t_{CLE}	20	—	—	ns	
Output valid from SCK low	t_{DO}	—	—	20	ns	
Output disable time	t_{DIS}	—	—	10	ns	**Note 1**

Note 1: This parameter is ensured by design and not 100% tested.

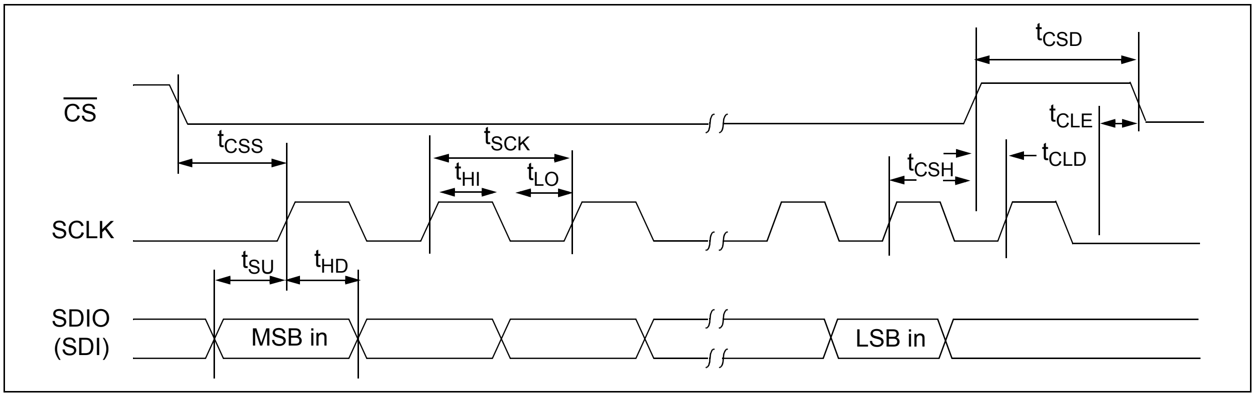


FIGURE 2-3: *SPI Serial Input Timing Diagram.*

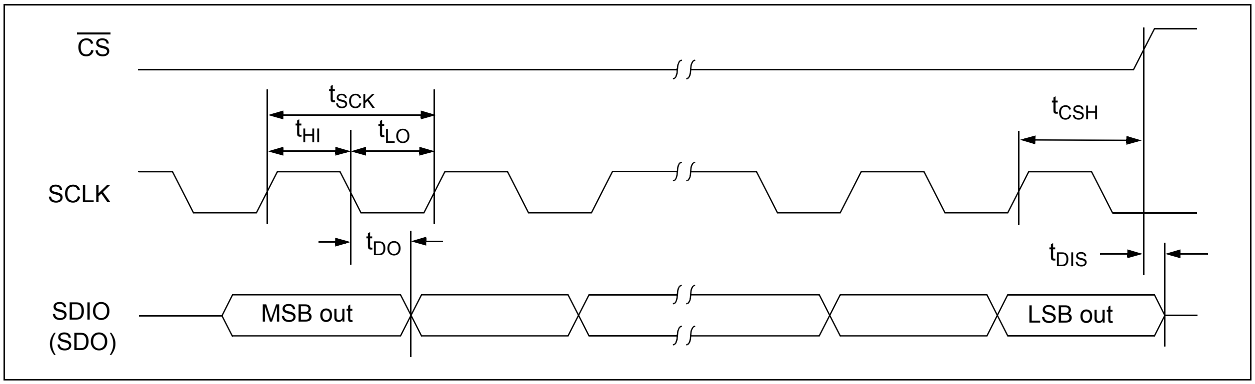


FIGURE 2-4: *SPI Serial Output Timing Diagram.*

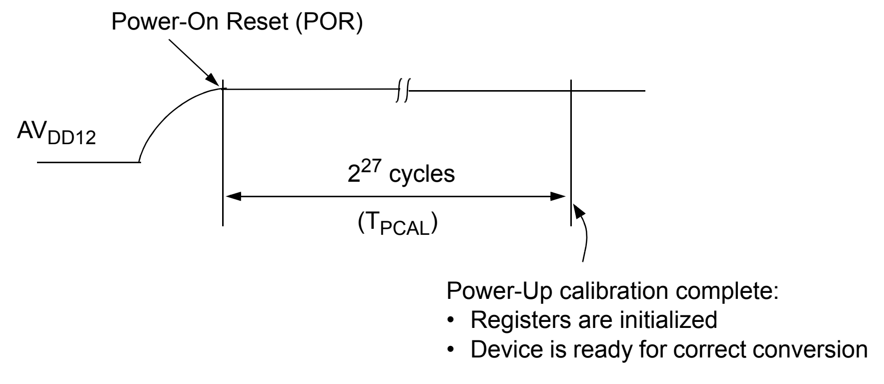


FIGURE 2-5: *POR-Related Events: Register Initialization and Power-Up Calibration.*

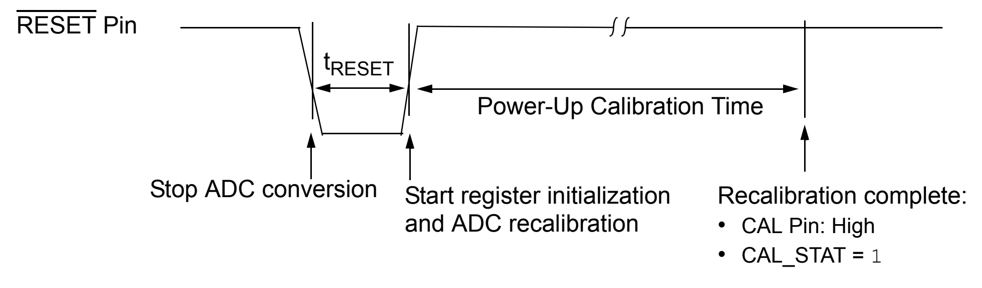


FIGURE 2-6: *$\overline{\text{RESET}}$ Pin Timing Diagram.*

TABLE 2-4: TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, AV_{DD18} = DV_{DD18} = 1.8V, AV_{DD12} = DV_{DD12} = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, DCLK_PHDLY_DEC<2:0> = `000`, Output load: CMOS data pin = 10 pF, LVDS = 100Ω termination, LVDS driver current setting = 3.5 mA, +25°C is applied for typical value.

Parameters		Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges (Note 1)							
Operating Temperature Range		T_A	-40	—	+85	°C	
Thermal Package Resistances (Note 2)							
121L Ball-TFBGA (8 mm x 8 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	40.2	—	°C/W	
	Junction-to-Case Thermal Resistance	θ_{JC}	—	8.4	—	°C/W	
124L VTLA (9 mm x 9 mm)	Junction-to-Ambient Thermal Resistance	θ_{JA}	—	21	—	°C/W	
	Junction-to-Case (top) Thermal Resistance	θ_{JC}	—	8.7	—	°C/W	

Note 1: Maximum allowed power dissipation (P_{DMAX}) = (T_{JMAX} – T_A)/θ_{JA}.

2: This parameter value is achieved by package simulations.

NOTES:

3.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, all parameters apply for T_A = -40°C to +85°C, $AV_{DD18} = DV_{DD18}$ = 1.8V, $AV_{DD12} = DV_{DD12}$ = 1.2V, GND = 0V, SENSE = AV_{DD12}, Single-channel mode, Differential analog input (A_{IN}) = -1 dBFS sine wave, f_{IN} = 70 MHz, Clock input = 200 MHz, f_S = 200 Msps (ADC core), PLL and decimation filters are disabled, 12-bit mode NSR if NSR is enabled.

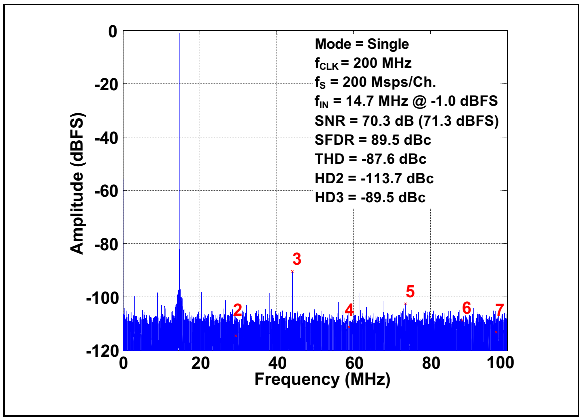


FIGURE 3-1: *FFT for 14.7 MHz Input Signal: f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.*

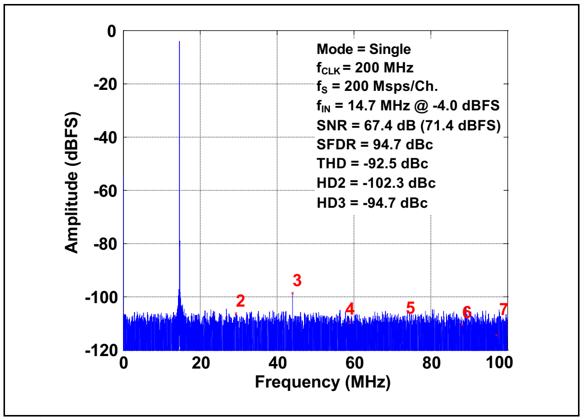


FIGURE 3-4: *FFT for 14.7 MHz Input Signal: f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.*

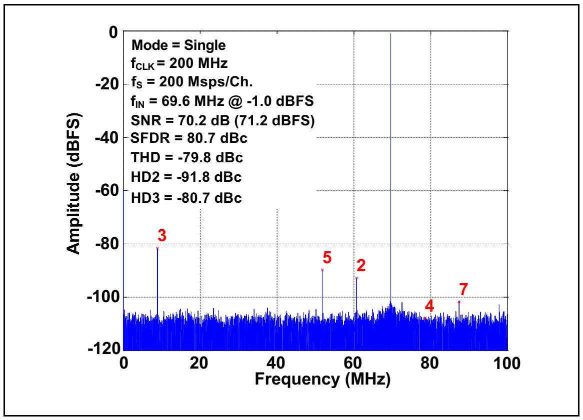


FIGURE 3-2: *FFT for 69.6 MHz Input Signal: f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.*

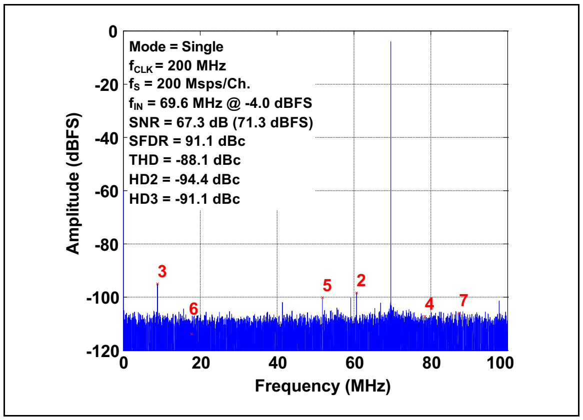


FIGURE 3-5: *FFT for 69.6 MHz Input Signal: f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.*

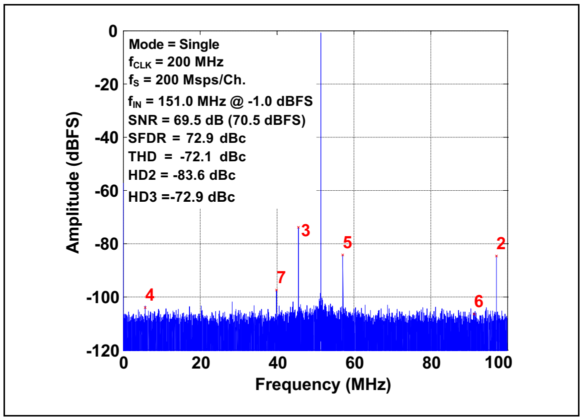


FIGURE 3-3: *FFT for 151 MHz Input Signal: Subsampled to 49 MHz, f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.*

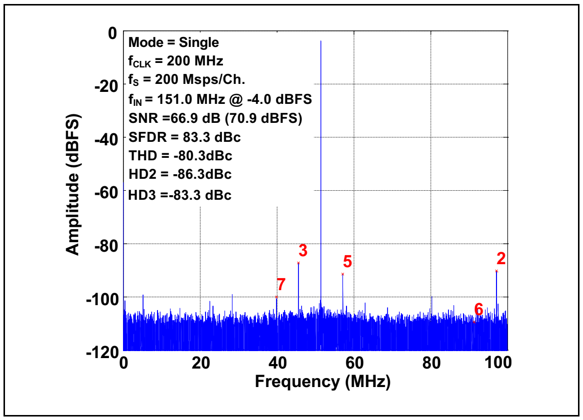


FIGURE 3-6: *FFT for 151 MHz Input Signal: Subsampled to 49 MHz, f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.*

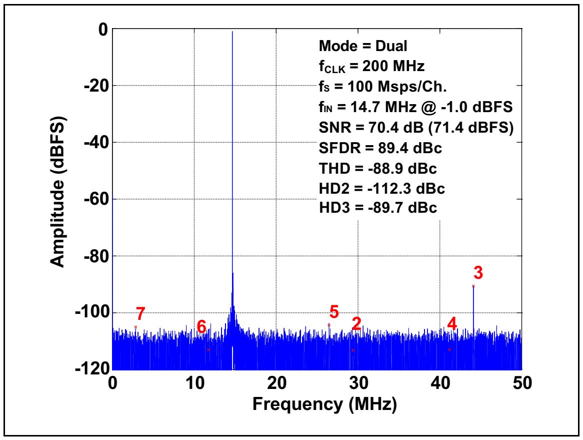


FIGURE 3-7: FFT for 14.7 MHz Input Signal: f_S = 100 Msps/Ch., Dual, A_{IN} = -1 dBFS.

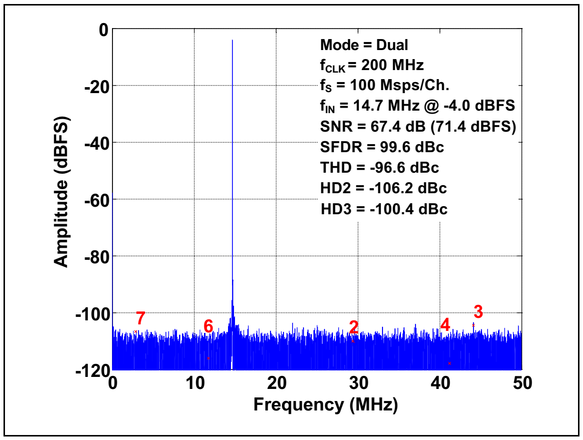


FIGURE 3-10: FFT for 14.7 MHz Input Signal: f_S = 100 Msps/Ch., Dual, A_{IN} = -4 dBFS.

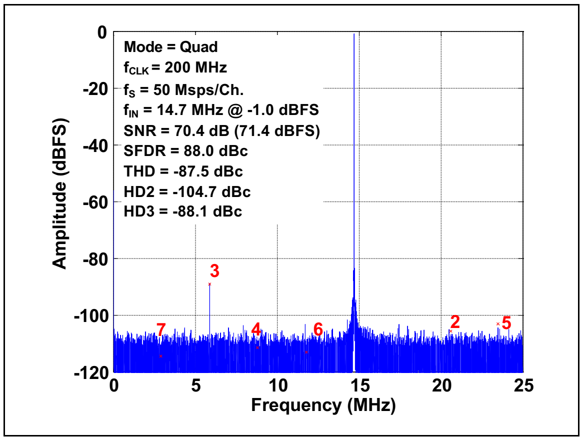


FIGURE 3-8: FFT for 14.7 MHz Input Signal: f_S = 50 Msps/Ch., Quad, A_{IN} = -1 dBFS.

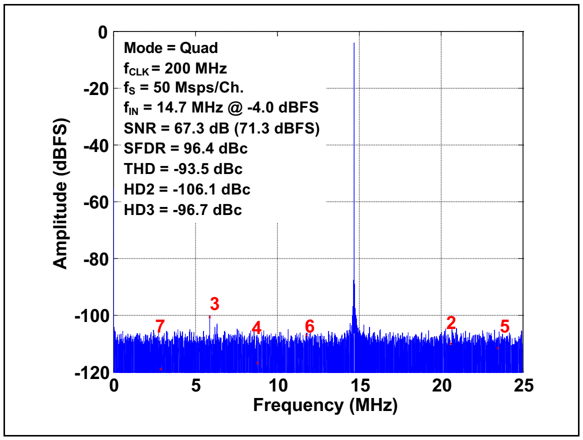


FIGURE 3-11: FFT for 14.7 MHz Input Signal: f_S = 50 Msps/Ch., Quad, A_{IN} = -4 dBFS.

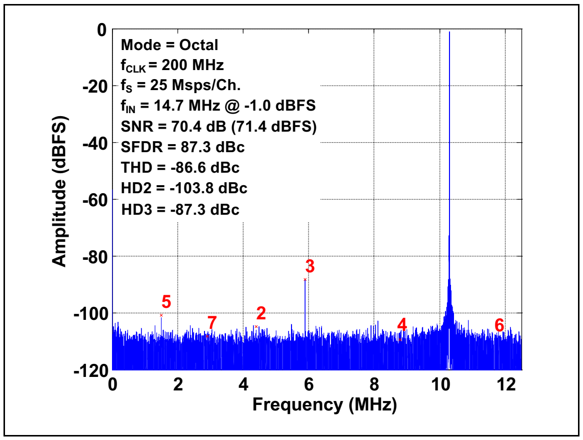


FIGURE 3-9: FFT for 14.7 MHz Input Signal: Subsampled to 10.3 MHz, f_S = 25 Msps/ Ch., Octal, A_{IN} = -1 dBFS.

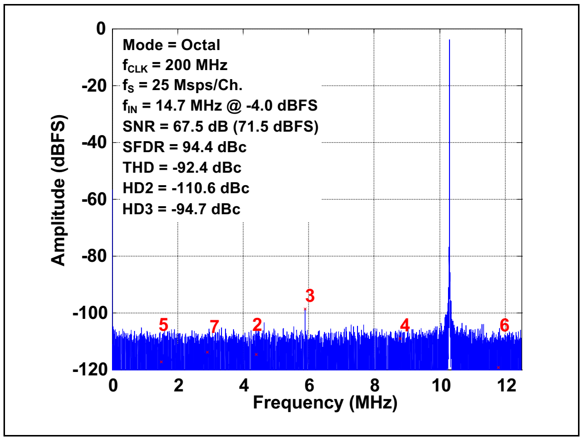


FIGURE 3-12: FFT for 14.7 MHz Input Signal: Subsampled to 10.3 MHz, f_S = 25 Msps/ Ch., Octal, A_{IN} = -4 dBFS.

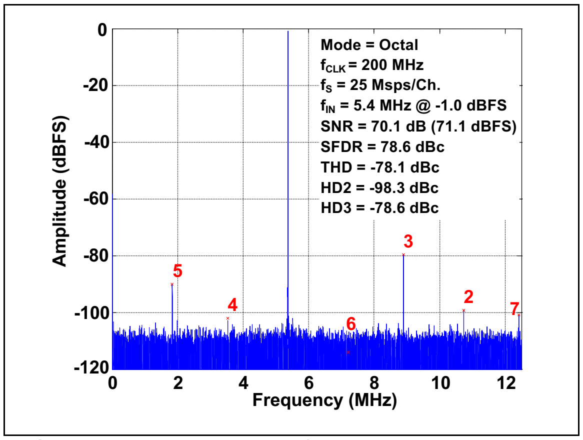


FIGURE 3-13: FFT for 69.6 MHz Input Signal: Subsampled to 5.4 MHz, f_S = 25 Msps/ Ch., Octal, A_{IN} = -1 dBFS.

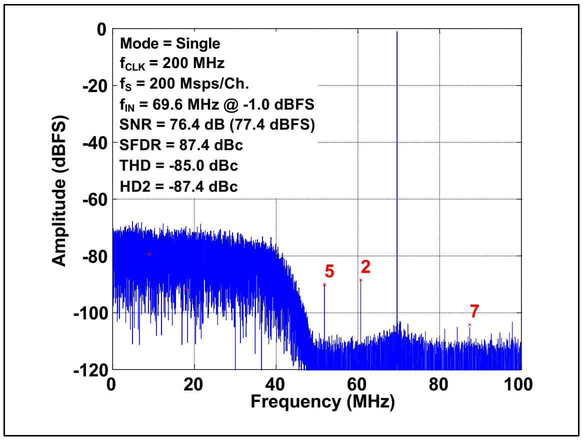


FIGURE 3-14: FFT for 69.6 MHz Input Signal with NSR enabled: NSR = 20, f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.

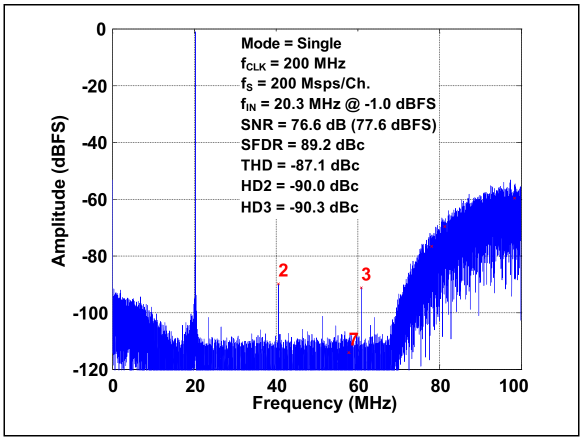


FIGURE 3-15: FFT for 20.3 MHz Input Signal with NSR enabled: NSR = 27, f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.

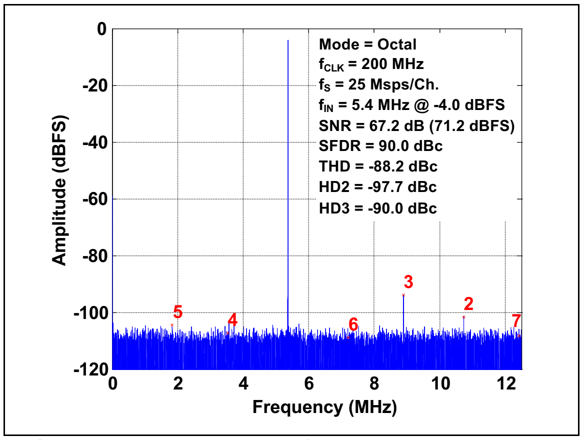


FIGURE 3-16: FFT for 69.6 MHz Input Signal: Subsampled to 5.4 MHz, f_S = 25 Msps/ Ch., Octal, A_{IN} = -4 dBFS.

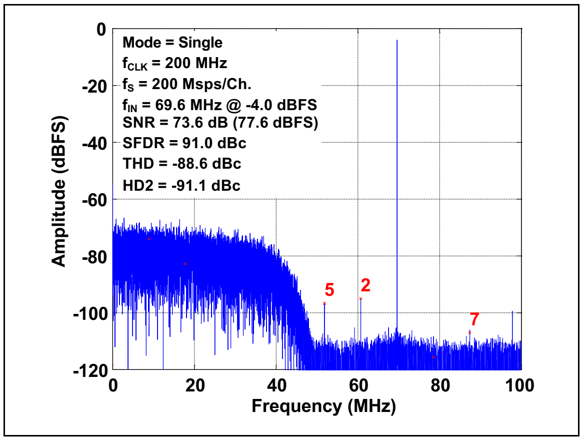


FIGURE 3-17: FFT for 69.6 MHz Input Signal with NSR enabled: NSR = 20, f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.

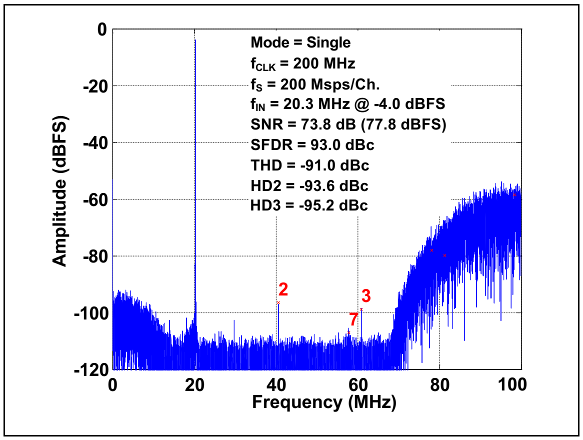


FIGURE 3-18: FFT for 20.3 MHz Input Signal with NSR enabled: NSR = 27, f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.

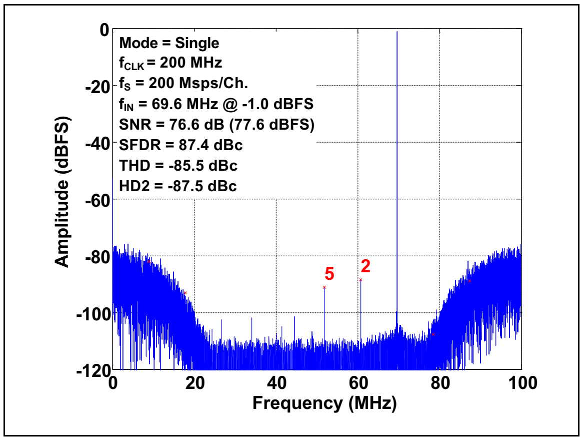


FIGURE 3-19: FFT for 69.6 MHz Input Signal with NSR enabled: NSR = 52, f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.

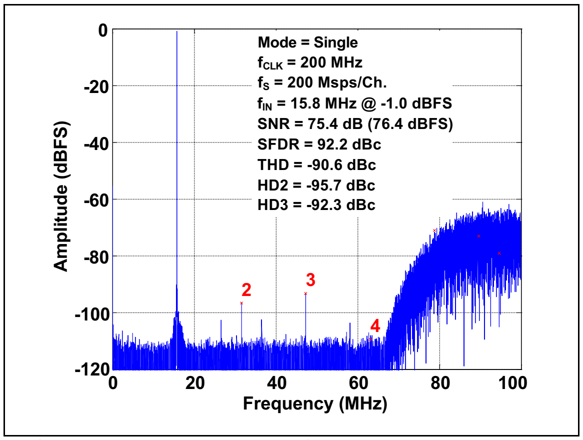


FIGURE 3-20: FFT for 15.8 MHz Input Signal with NSR enabled: NSR = 63, f_S = 200 Msps/Ch., A_{IN} = -1 dBFS.

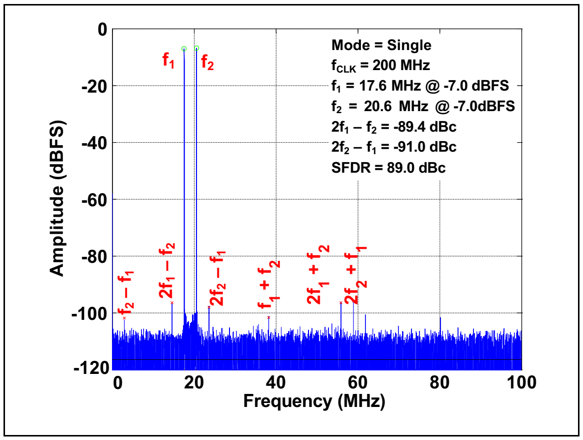


FIGURE 3-21: Two-Tone FFT: f_{IN1} = 17.6 MHz and f_{IN2} = 20.6 MHz, A_{IN} = -7 dBFS per Tone, f_S = 200 Msps.

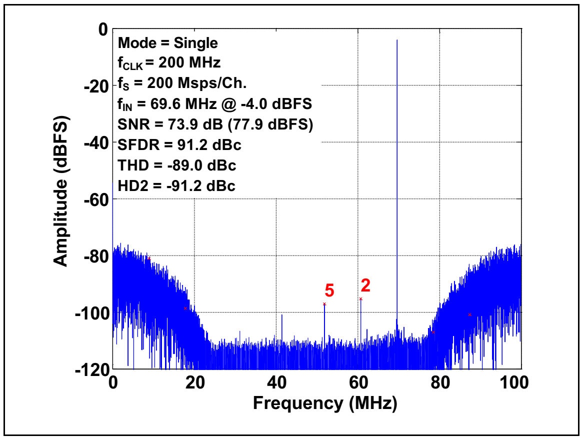


FIGURE 3-22: FFT for 69.6 MHz Input Signal with NSR enabled: NSR = 52, f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.

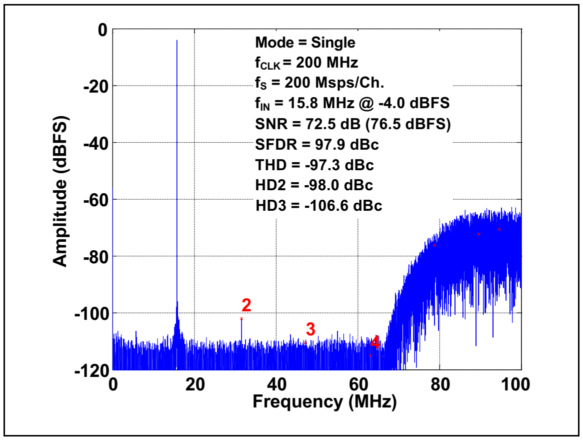


FIGURE 3-23: FFT for 15.8 MHz Input Signal with NSR enabled: NSR = 63, f_S = 200 Msps/Ch., A_{IN} = -4 dBFS.

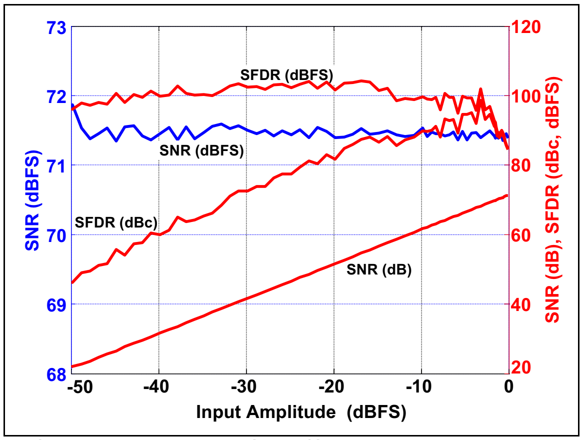


FIGURE 3-24: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 15 MHz, High-Reference Mode (SENSE = AV_{DD12}).

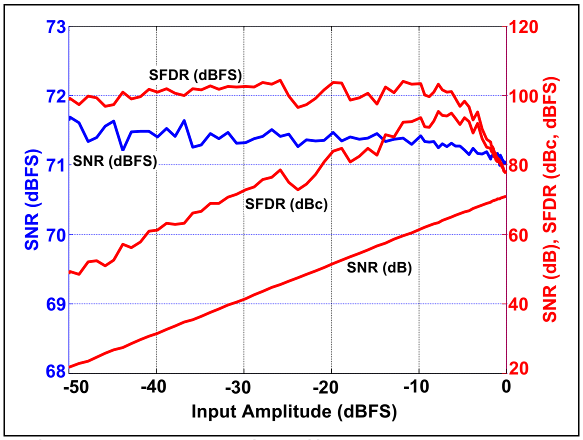


FIGURE 3-27: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 70 MHz, High-Reference Mode (SENSE = AV_{DD12}).

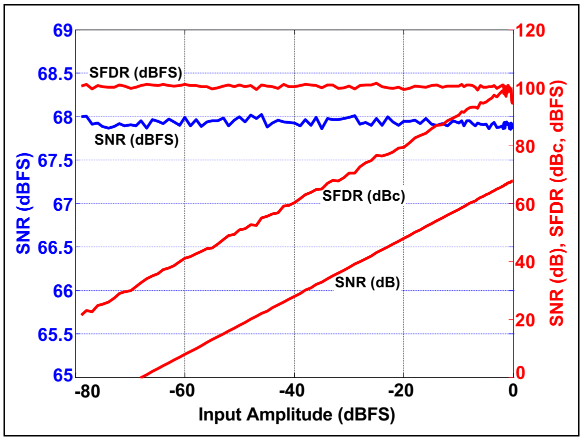


FIGURE 3-25: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 15 MHz, Low-Reference Mode (SENSE = GND).

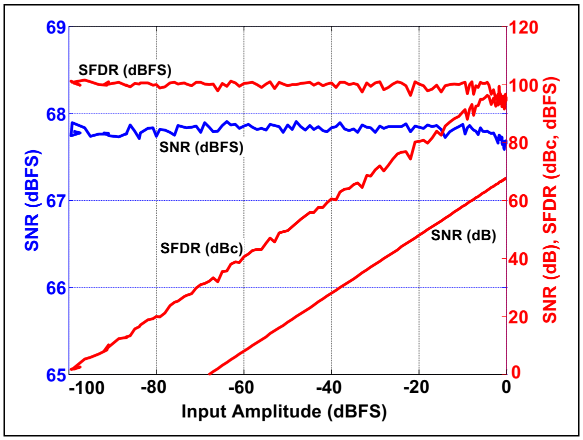


FIGURE 3-28: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 70 MHz, Low-Reference Mode (SENSE = GND).

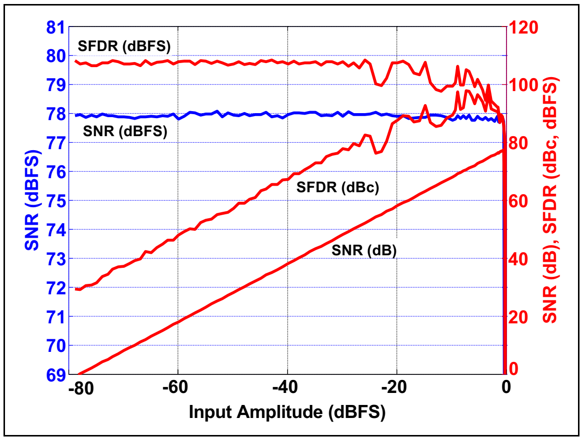


FIGURE 3-26: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 15 MHz, High-Reference Mode (SENSE = AV_{DD12}) with NSR enabled. $A_{IN} \leq$ 0.8 dBFS for NSR. Noise is calculated within the NSR bandwidth (25% of sampling frequency).

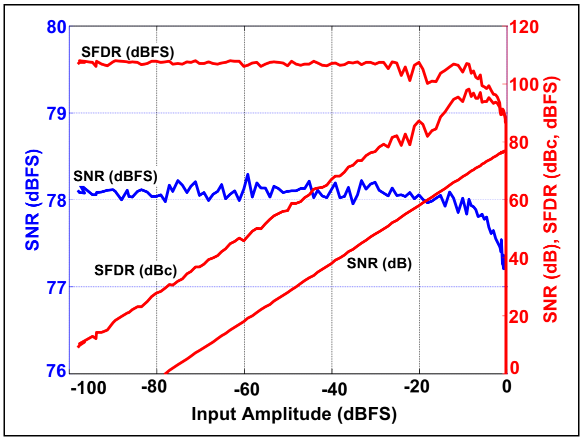


FIGURE 3-29: SNR/SFDR vs. Analog Input Amplitude: f_S = 200 Msps, f_{IN} = 70 MHz, High-Reference Mode (SENSE = AV_{DD12}) with NSR enabled. $A_{IN} \leq$ 0.8 dBFS for NSR. Noise is calculated within the NSR bandwidth (25% of sampling frequency).

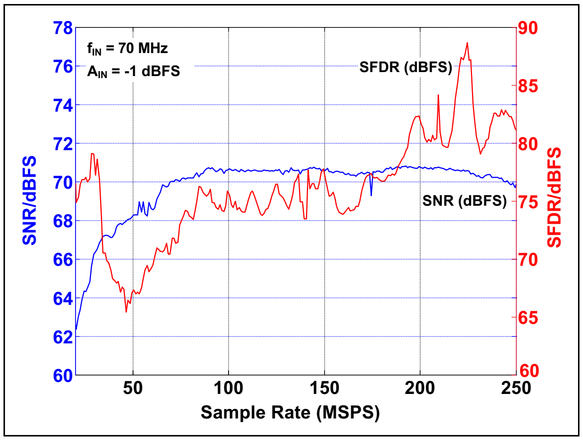


FIGURE 3-30: *SNR/SFDR vs. Sample Rate (Msps): f_{IN} = 70 MHz.*

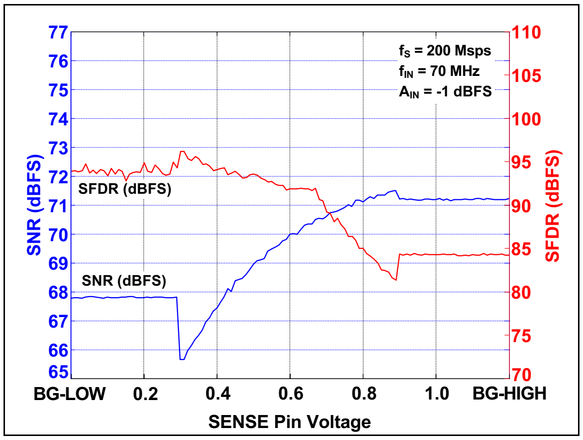


FIGURE 3-31: *SNR/SFDR vs. SENSE Pin Voltage: f_S = 200 Msps, f_{IN} = 70 MHz.*

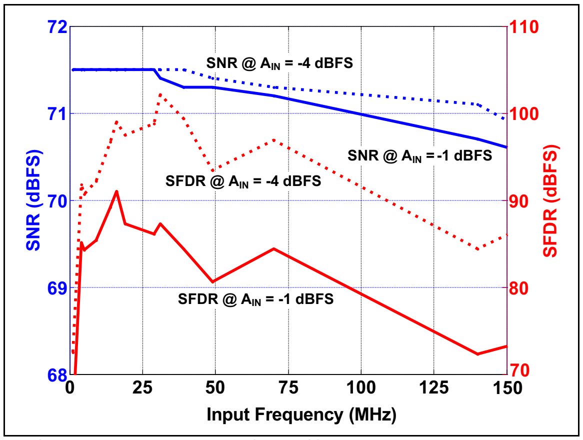


FIGURE 3-32: *SNR/SFDR vs. Input Frequency.*

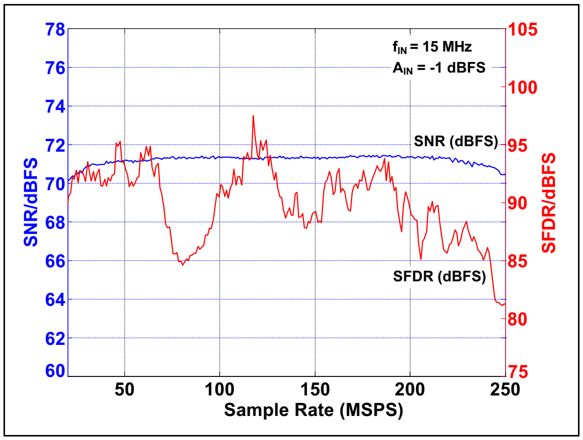


FIGURE 3-33: *SNR/SFDR vs. Sample Rate (Msps): f_{IN} = 15 MHz.*

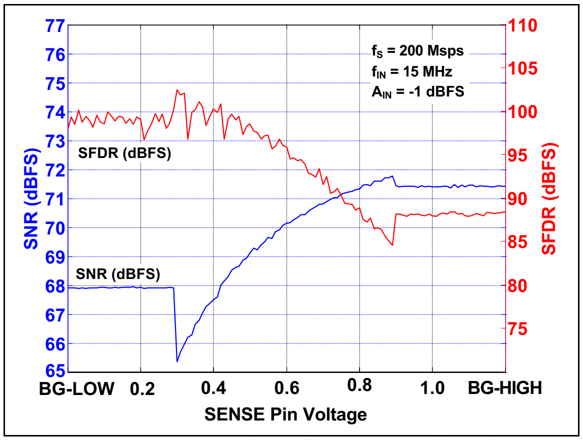


FIGURE 3-34: *SNR/SFDR vs. SENSE Pin Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

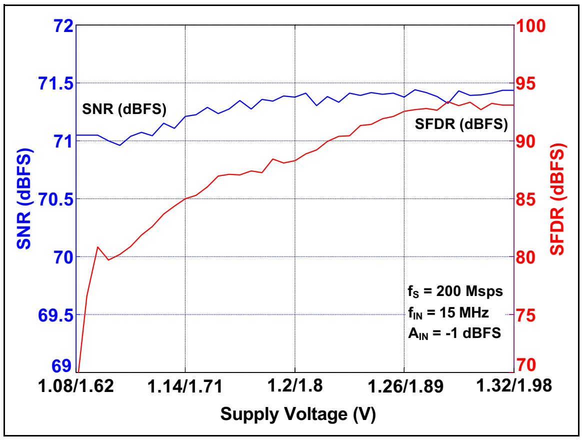


FIGURE 3-35: *SNR/SFDR vs. Supply Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

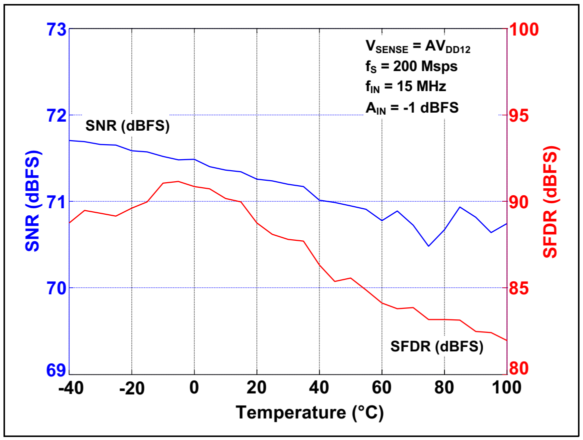


FIGURE 3-36: *SNR/SFDR vs. Temperature: f_S = 200 Msps, f_{IN} = 15 MHz.*

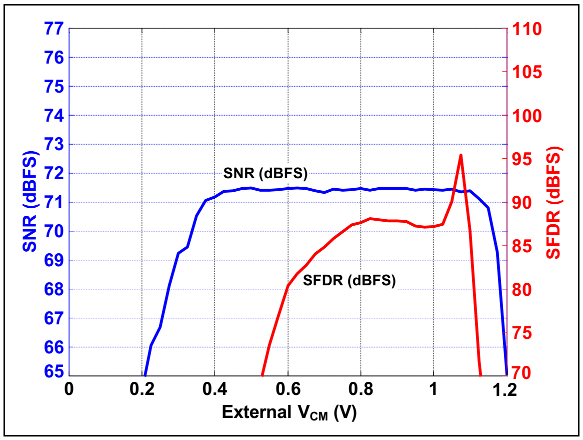


FIGURE 3-37: *SNR/SFDR vs. V_{CM} Voltage (Externally Applied): f_S = 200 Msps, f_{IN} = 15 MHz.*

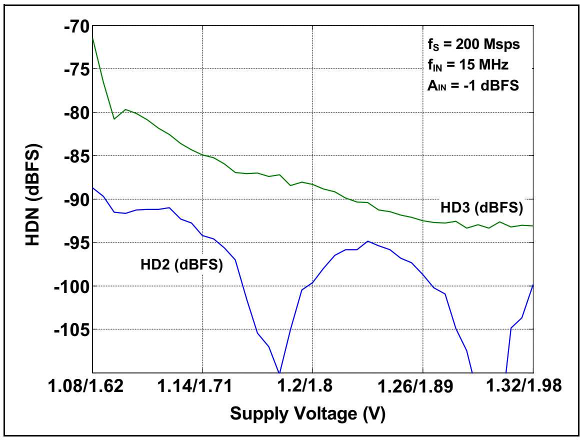


FIGURE 3-38: *HD2/HD3 vs. Supply Voltage: f_S = 200 Msps, f_{IN} = 15 MHz.*

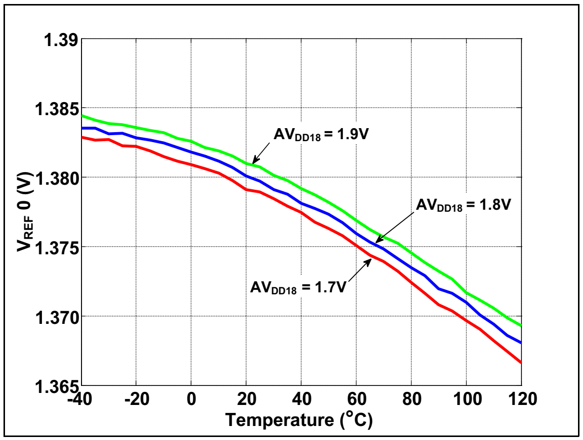


FIGURE 3-39: *V_{REF0} vs. Temperature.*

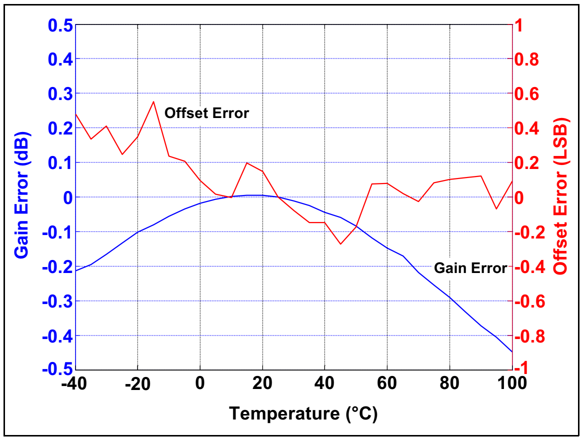


FIGURE 3-40: *Gain and Offset Error Drifts vs. Temperature Using Internal Reference, with Respect to 25°C: f_S = 200 Msps.*

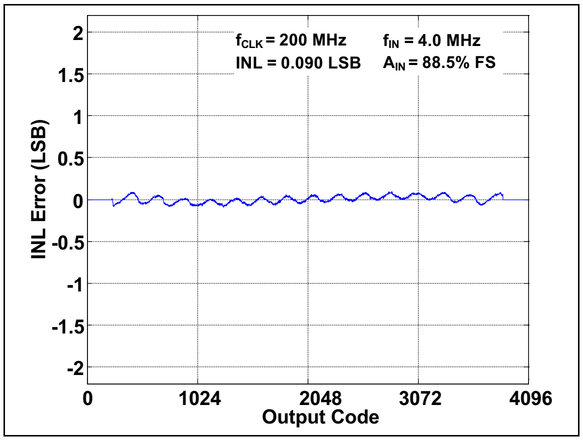


FIGURE 3-41: *INL Error vs. Output Code: f_S = 200 Msps, f_{IN} = 4 MHz.*

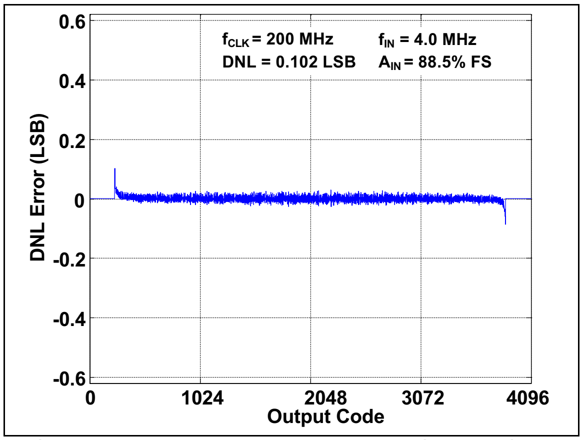


FIGURE 3-42: *DNL Error vs. Output Code: f_S = 200 Msps, f_{IN} = 4 MHz.*

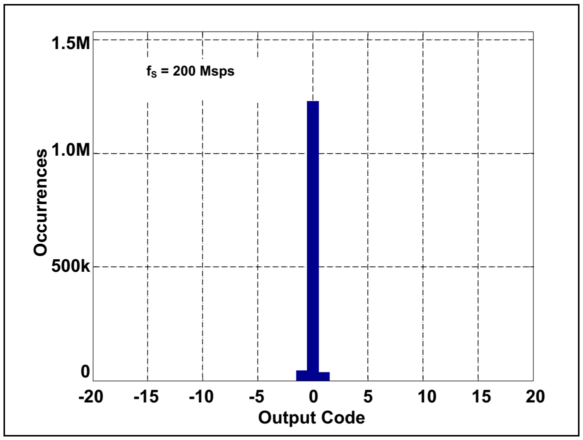


FIGURE 3-43: *Shorted Input Histogram.*

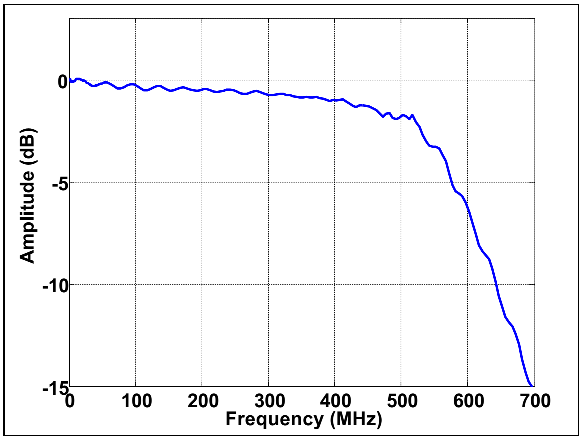


FIGURE 3-44: *Input Bandwidth.*

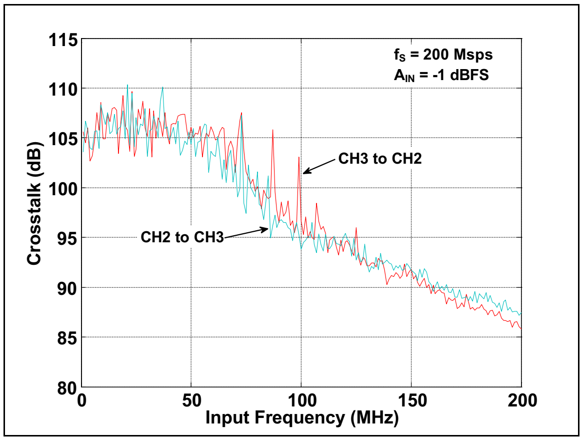


FIGURE 3-45: *Input Channel Crosstalk.*

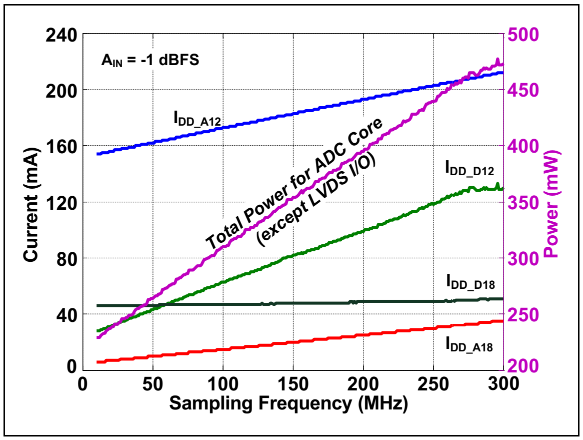


FIGURE 3-46: *Power Consumption vs. Sampling Frequency (LVDS Mode).*

4.0 THEORY OF OPERATION

The MCP37211-200 and MCP37D11-200 device family is a low-power, 12-bit, 200 Msps analog-to-digital converter (ADC) with built-in features, including harmonic distortion correction (HDC), DAC noise cancellation (DNC), dynamic element matching (DEM) and flash error calibration.

The devices offer various built-in digital signal post-processing features. Both the MCP37211-200 and MCP37D11-200 offer high-order FIR digital decimation filters, noise-shaping requantizer (NSR), gain and offset adjustment per channel and fractional delay recovery (FDR). The MCP37D11-200 includes additional features such as digital down-conversion (DDC) and CW beamforming capability. These built-in advanced digital signal post-processing sub-blocks, which are individually controlled using configuration register bit settings, can be used for various special applications such as I/Q demodulation, digital down-conversion and ultrasound imaging.

The device's operational modes and feature sets are configured using the user-programmable internal registers. All user registers, except for the factory-controlled registers, are reprogrammable using the SPI interface. When the device is first powered up, the device is running with default settings. The user can select external clock input or on-board phase lock loop (PLL) output as the input sampling frequency by setting the clock source selection bit. In multi-channel mode, the input channel selection and MUX scan order are user-configurable and the inputs are sequentially multiplexed by the input MUX defined by the scan order.

The device samples the analog input on the rising edge of the clock. The digital output code is available after 28 clock cycles of data latency. Latency will increase if any of the digital signal post-processing (DSPP) options are enabled.

The output data can be coded in two's complement or offset binary format and randomized using the user option. Data can be output using either the CMOS or double data rate (DDR) LVDS (Low Voltage Differential Signaling) interface.

4.1 ADC Core Architecture

Figure 4-1 shows the simplified block diagram of the ADC core. The first stage consists of a 17-level flash ADC, a multi-level digital-to-analog converter (DAC) and a residue amplifier with a gain of 8. Stages 2 to 6 consist of a 9-level (3-bit) flash ADC, a multi-level DAC and a residue amplifier with a gain of 4. The last stage is a 9-level 3-bit flash ADC. Dither is added in each of the first three stages.The digital outputs from all seven stages are combined in a digital error correction logic block and digitally processed for the final output.

The first three stages include patented digital calibration features:

- Harmonic Distortion Correction (HDC) algorithm that digitally measures and cancels ADC errors arising from distortions introduced by the residue amplifiers
- DAC Noise Cancellation (DNC) algorithm that corrects DAC's nonlinearity errors
- Dynamic Element Matching (DEM) which randomizes DAC errors thereby converting harmonic distortion to white noise

These digital correction algorithms are first applied during the power-on reset sequence and then operate in the background during normal operation of the pipelined ADC. These algorithms automatically track and correct any environmental changes in the ADC.

More details of the system correction algorithms are shown in **Section 4.16 "System Calibration"**.

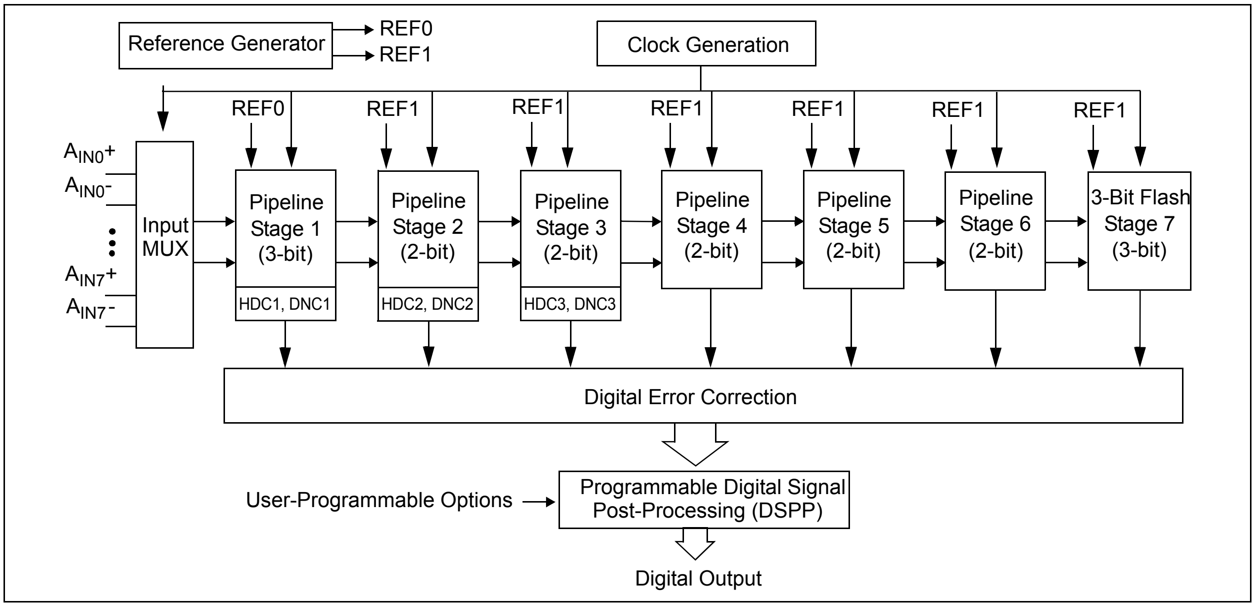


FIGURE 4-1: *ADC Core Block Diagram.*

4.2 Supply Voltage (DV_{DD}, AV_{DD}, GND)

The device operates from two sets of supplies and a common ground:

- Digital Supplies (DV_{DD}) for the digital section: 1.8V and 1.2V
- Analog Supplies (AV_{DD}) for the analog section: 1.8V and 1.2V
- Ground (GND): common ground for both digital and analog sections

The supply pins require an appropriate bypass capacitor (ceramic) to attenuate high-frequency noise present in most application environments. The ground pins provide the current return path. These ground pins must connect to the ground plane of the PCB through a low-impedance connection. A ferrite bead can be used to separate analog and digital supply lines if a common power supply is used for both analog and digital sections.

4.3 Input Sample Rate

In single-channel mode, the device samples the input at full speed. In multi-channel mode, the core ADC is multiplexed between the selected channels. The resulting effective sample rate per channel is given by:

EQUATION 4-1: SAMPLE RATE PER CHANNEL

$$\text{Sample Rate/Channel} = \frac{\text{Full ADC Sample Rate}(fs)}{\text{Number of Channel Used}}$$

For example, with 200 Msps operation, the input is sampled at the full 200 Msps rate if a single channel is used or at 25 Msps per channel if all eight channels are used.

4.4 Analog Input Channel Selection

The analog input is auto-multiplexed sequentially as defined by the channel-order selection bit setting. The user can configure the input MUX using the following registers:

- SEL_NCH<2:0> in Address 0x01 (Register 5-2): select the total number of input channels to be used
- Address 0x7D – 0x7F (Registers 5-38 – 5-40): select auto-scan channel order

The user can select up to eight input channels. If all eight input channels are to be used, SEL_NCH<2:0> is set to `000` and the input channel sampling order is set using Addresses 0x7D – 0x7F.

Regardless of how many channels are selected, all eight channels must be programmed in Addresses 0x7D – 0x7F without duplication: program the addresses of the selected channels in sequential order followed by unused channels. The order of unused channels has no meaning. The device samples the first N-Channels listed in Addresses 0x7D – 0x7F sequentially, where N is the total number of channels to be used, defined by the SEL_NCH<2:0>. Table 4-1 shows examples of input channel selection using Addresses 0x7D – 0x7F.

TABLE 4-1: EXAMPLE: CHANNEL ORDER SELECTION USING ADDRESSES 0X7D – 0X7F

No. of Channels (Note 1)	Selected Channels	Channel Order (Note 2)	Address 0x7F								Address 0x7E								Address 0x7D							
			b 7							b 0	b 7							b 0	b 7							b 0
8			Channel Order Bit Settings																							
			5th Ch.			4th Ch.			6th Ch.			3rd Ch.			7th Ch.			2nd Ch.			8th Ch.			1st Ch.		
	[0 1 2 3 4 5 6 7]	[0 1 2 3 4 5 6 7] (Default)	1	0	0	0	1	1	1	0	1	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0
	[7 6 5 4 3 2 1 0]	[7 6 5 4 3 2 1 0]	0	1	1	1	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	1	1	1
	[0 2 4 6 1 3 5 7]	[0 2 4 6 1 3 5 7]	0	0	1	1	1	0	0	1	1	1	0	0	1	0	1	0	1	0	1	1	1	0	0	0
	[1 3 5 7 0 2 4 6]	[1 3 5 7 0 2 4 6]	0	0	0	1	1	1	0	1	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0	1

Note 1: Defined by SEL_NCH<2:0> in Address 0x01 (Register 5-2).

2: Individual channel order should not be repeated. Unused channels are still assigned after the selected channel address. The order of the unused channel address has no meaning since they are not used.

TABLE 4-1: EXAMPLE: CHANNEL ORDER SELECTION USING ADDRESSES 0X7D – 0X7F

No. of Channels (Note 1)	Selected Channels	Channel Order (Note 2)	Address 0x7F								Address 0x7E								Address 0x7D							
			b7							b0	b7							b0	b7							b0
7			Channel Order Bit Settings																							
			Unused			4th Ch.			5th Ch.			3rd Ch.			6th Ch.			2nd Ch.			7th Ch.			1st Ch.		
	[0 1 2 3 4 5 6]	[0 1 2 3 4 5 6 7]	1	1	1	0	1	1	1	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0
	[0 2 4 6 1 3 5]	[0 2 4 6 1 3 5 7]	1	1	1	1	1	0	0	0	1	1	0	0	0	1	1	0	1	0	1	0	1	0	0	0
6			Channel Order Bit Settings																							
			Unused			Unused			4th Ch.			3rd Ch.			5th Ch.			2nd Ch.			6th Ch.			1st Ch.		
	[0 1 2 3 4 5]	[0 1 2 3 4 5 6 7]	1	1	1	1	1	0	0	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0
	[0 2 4 6 1 3]	[0 2 4 6 1 3 5 7]	1	1	1	1	0	1	1	1	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0
5			Channel Order Bit Settings																							
			Unused			Unused			Unused			3rd Ch.			4th Ch.			2nd Ch.			5th Ch.			1st Ch.		
	[0 1 2 3 4]	[0 1 2 3 4 5 6 7]	1	1	0	1	0	1	1	1	1	0	1	0	0	1	1	0	0	1	1	0	0	0	0	0
	[0 2 4 6 1]	[0 2 4 6 1 3 5 7]	1	0	1	0	1	1	1	1	1	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0
4			Channel Order Bit Settings																							
			Unused			Unused			Unused			Unused			3rd Ch.			2nd Ch.			4th Ch.			1st Ch.		
	[0 1 2 3]	[0 1 2 3 4 5 6 7]	1	1	0	1	0	1	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	0	0	0
	[4 5 6 7]	[4 5 6 7 0 1 2 3]	0	1	0	0	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1	1	1	1	0	0
	[0 2 4 6]	[0 2 4 6 1 3 5 7]	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0	0	1	0	1	1	0	0	0	0
	[1 3 5 7]	[1 3 5 7 0 2 4 6]	1	0	0	0	1	0	1	1	0	0	0	0	1	0	1	0	1	1	1	1	1	0	0	1
3			Channel Order Bit Settings																							
			Unused			Unused			Unused			Unused			Unused			2nd Ch.			3rd Ch.			1st Ch.		
	[0 1 2]	[0 1 2 3 4 5 6 7]	1	0	1	1	0	0	1	1	0	0	1	1	1	1	1	0	0	1	0	1	0	0	0	0
	[0 2 4]	[0 2 4 6 1 3 5 7]	0	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	1	0	1	0	0	0	0	0
2			Channel Order Bit Settings																							
			Unused			Unused			Unused			Unused			Unused			Unused			2nd Ch.			1st Ch.		
	[0 1]	[0 1 2 3 4 5 6 7]	1	0	1	1	0	0	1	1	0	0	1	1	1	1	1	0	1	0	0	0	1	0	0	0
	[2 3]	[2 3 0 1 4 5 6 7]	1	0	1	1	0	0	1	1	0	0	0	1	1	1	1	0	0	0	0	1	1	0	1	0
	[4 5]	[4 5 0 1 2 3 6 7]	0	1	1	0	1	0	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1	1	0	0
	[6 7]	[6 7 0 1 2 3 4 5]	0	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1	1	0
1			Channel Order Bit Settings																							
			Unused			Unused			Unused			Unused			Unused			Unused			Unused			1st Ch.		
	[0]	[0 1 2 3 4 5 6 7]	1	0	0	0	1	1	1	0	1	0	1	0	1	1	0	0	0	1	1	1	1	0	0	0
	[1]	[1 0 2 3 4 5 6 7]	1	0	0	0	1	1	1	0	1	0	1	0	1	1	0	0	0	0	1	1	1	0	0	1
	[2]	[2 0 1 3 4 5 6 7]	1	0	0	0	1	1	1	0	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1	0
	[3]	[3 0 1 2 4 5 6 7]	1	0	0	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	1	1	1	0	1	1
	[4]	[4 0 1 2 3 5 6 7]	0	1	1	0	1	0	1	0	1	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0
	[5]	[5 0 1 2 3 4 6 7]	0	1	1	0	1	0	1	0	0	0	0	1	1	1	0	0	0	0	1	1	1	1	0	1
	[6]	[6 0 1 2 3 4 5 7]	0	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	1	1	1	1	0
	[7]	[7 0 1 2 3 4 5 6]	0	1	1	0	1	0	1	0	0	0	0	1	1	0	1	0	0	0	1	1	0	1	1	1

Note 1: Defined by SEL_NCH<2:0> in Address 0x01 (Register 5-2).

2: Individual channel order should not be repeated. Unused channels are still assigned after the selected channel address. The order of the unused channel address has no meaning since they are not used.

4.5 Analog Input Circuit

The analog input of the MCP37211-200 and MCP37D11-200 is a differential CMOS switched capacitor sample-and-hold circuit. Figure 4-2 shows the equivalent input structure of the device.

The input impedance of the device is mostly governed by the input sampling capacitor (C_S = 6 pF) and input sampling frequency (f_S). The performance of the device can be affected by the input signal conditioning network (see Figure 4-3). The analog input signal source must have sufficiently low output impedance to charge the sampling capacitors (C_S = 6 pF) within one clock cycle. A small external resistor (e.g., 5Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low-pass filter with the capacitor and their values must be determined by application requirements and input frequency.

The V_{CM} pin provides a common-mode voltage reference (0.9V), which can be used for a center-tap voltage of an RF transformer or balun. If the V_{CM} pin voltage is not used, the user may create a common mode voltage at mid-supply level ($AV_{DD18}/2$).

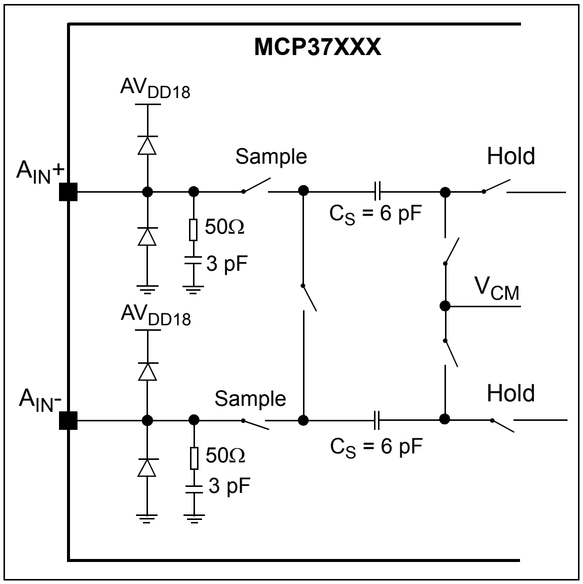


FIGURE 4-2: *Equivalent Input Circuit.*

4.5.1 ANALOG INPUT DRIVING CIRCUIT

4.5.1.1 Differential Input Configuration

The device achieves optimum performance when the input is driven differentially, where common-mode noise immunity and even-order harmonic rejection are significantly improved. If the input is single-ended, it must be converted to a differential signal in order to properly drive the ADC input. The differential conversion and common mode application can be accomplished by using an RF transformer or balun with a center-tap. Additionally, one or more anti-aliasing filters may be added for optimal noise performance and should be tuned such that the corner frequency is appropriate for the system.

Figure 4-3 shows an example of the differential input circuit with transformer. Note that the input driving circuits are terminated by 50Ω near the ADC side through a pair of 25Ω resistors from each input to the common-mode (V_{CM}) from the device. The RF transformer must be carefully selected to avoid artificial high harmonic distortion. The transformer can be damaged due to excessive input power or due to an RF input being applied while the MCP37XXX is powered off. Figure 4-4 shows an input configuration example when a differential output amplifier is used.

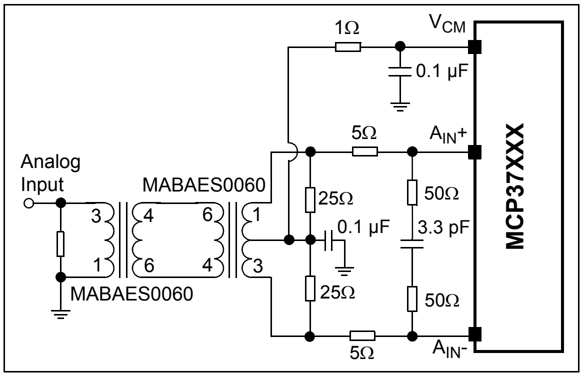


FIGURE 4-3: *Transformer Coupled Input Configuration.*

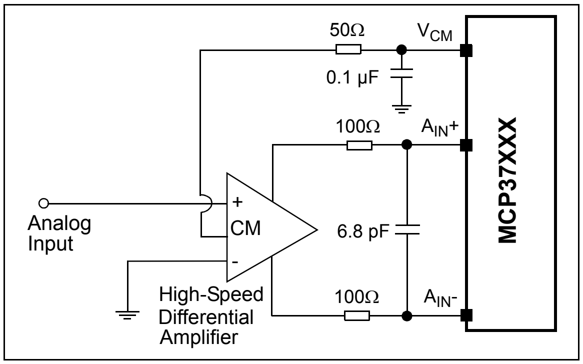


FIGURE 4-4: *DC-Coupled Input Configuration with Preamplifier: the external signal conditioning circuit and associated component values are for reference only. Typically, the amplifier manufacturer provides reference circuits and component values.*

4.5.1.2 Single-Ended Input Configuration

SNR and SFDR performance degrades significantly when the device is operated in a single-ended configuration. The unused negative side of the input should be AC-coupled to ground using a capacitor. Figure 4-5 shows an example of a single-ended input configuration.

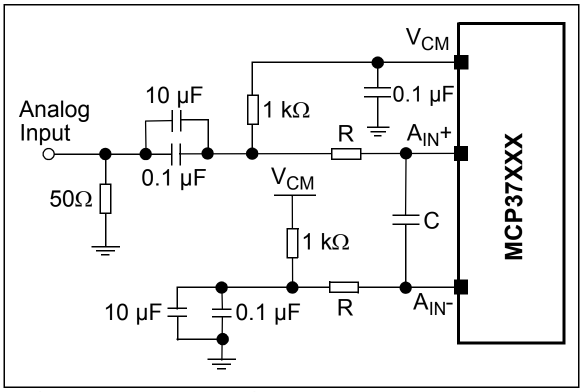
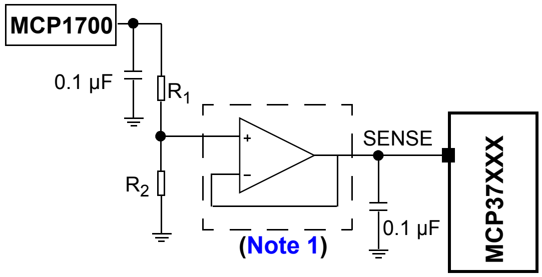


FIGURE 4-5: Singled-Ended Input Configuration.

4.5.2 SENSE VOLTAGE AND INPUT FULL-SCALE RANGE

The device has a bandgap-based differential internal reference voltage. The SENSE pin voltage is used to select the internal reference voltage source and configures the input full-scale range. A comparator detects the SENSE pin voltage and configures the full-scale input range into one of the three possible modes which are summarized in Table 4-2. Figure 4-6 shows an example of how the SENSE pin should be driven.

The SENSE pin can sink or source currents as high as 500 µA across all operational conditions. Therefore, it may require a driver circuit, unless the SENSE reference source provides sufficient output current.



Note 1: This voltage buffer can be removed if SENSE reference is coming from a stable source (such as MCP1700) which can provide a sufficient output current to the SENSE pin.

FIGURE 4-6: SENSE Pin Voltage Setup.

TABLE 4-2: SENSE PIN VOLTAGE AND INPUT FULL-SCALE RANGE

SENSE Pin Voltage (V_{SENSE})	Selected Reference Voltage (V_{REF})	Full-Scale Input Voltage Range (A_{FS})	Condition
Tied to GND	0.74375V	1.4875 V_{P-P} (Note 1)	Low-Reference Mode (Note 4)
0.4V – 0.8 V	0.74375V – 1.4875V	1.4875 V_{P-P} to 2.975 V_{P-P} (Note 2)	Sense Mode (Note 5)
Tied to AV_{DD12}	1.4875V	2.975 V_{P-P} (Note 3)	High-Reference Mode (Note 4)

Note 1: A_{FS} = (17/16) x 1.4 V_{P-P} = 1.487 V_{P-P}.
2: A_{FS} = (17/16) x 2.8 V_{P-P} x (V_{SENSE})/0.8 = 1.4875 V_{P-P} to 2.975 V_{P-P}.
3: A_{FS} = (17/16) x 2.8 V_{P-P} = 2.975 V_{P-P}.
4: Based on internal bandgap voltage.
5: Based on V_{SENSE}.

4.5.3 SNR/SFDR PERFORMANCE VS. SENSE SELECTION

The SENSE pin is used to configure the full-scale input range of the ADC. Depending on the application conditions, the SNR, SFDR and dynamic range performance are affected by the SENSE pin configuration and also by the Noise-Shaping Requantizer (NSR) option. Table 4-3 summarizes these options.

TABLE 4-3: SENSE AND NSR OPTION VS. SNR/SFDR PERFORMANCE

SENSE and NSR	Descriptions
High-Reference Mode (SENSE pin = AV_{DD12})	Optimizes SNR, high input full-scale range, but may require external dither (i.e., random noise) for input signals with very low amplitude
Low-Reference Mode (SENSE pin = ground)	Optimizes dynamic range and SFDR, but reduces SNR
Sense Mode (SENSE pin = 0.4V to 0.8V)	Allows dynamic trade-off between High-Reference and Low-Reference modes
Noise-Shaping Requantizer (NSR)	Optimizes SNR, but reduces usable bandwidth NSR can be employed in any SENSE pin configuration

4.5.3.1 Using High-Reference Mode

This mode is enabled by setting the SENSE pin to AV_{DD12} (1.2V).

This mode provides the highest input full-scale range (2.975 V_{P-P}) and the highest SNR performance. In this mode, the internal thermal noise is less than 1 LSB of the 12-bit ADC (726 µV or -72 dBFS). This has the consequence of making it difficult to resolve small input signals unless some dither is added to the ADC input. In typical applications, thermal noise generated by the system driving the ADC will provide the necessary dithering effect.

Figures 3-24 and 3-27 show SNR/SFDR versus input amplitude in High-Reference mode.

Note: Adding dither to the ADC has the negative side effect of reducing the maximum achievable SNR.

4.5.3.2 Using Low-Reference Mode

This mode is enabled by setting the SENSE pin to ground.

For applications which require a large dynamic range but are able to sacrifice a small amount of SNR or for applications which desire a smaller input signal range and improved SFDR characteristics, the Low-Reference mode is recommended. In this mode, the input full-scale range and hence the LSB size are reduced to ½ of the High-Reference mode. Therefore, the thermal noise of the ADC acts as an effective dither source to allow signal measurements well below the 1 LSB level. In this mode, however, the thermal noise becomes a dominant noise source and therefore the maximum achievable SNR is reduced by 3 dB from what is achievable with the High-Reference mode and by 7 dB from what is achievable with NSR mode.

Figures 3-25 and 3-28 show SNR/SFDR versus input amplitude in Low-Reference mode.

4.5.3.3 Using SENSE Mode

This mode is enabled by driving the SENSE pin with an external voltage source between 0.4V and 0.8V.

This mode allows the user to adjust the input full-scale range such that SNR and dynamic range are optimized in a given application system environment.

4.5.3.4 Using NSR Mode

The use of the Noise-Shaping Requantizer (NSR), further described in **Section 4.8.2 “Noise-Shaping ReQuantizer (NSR)”**, is best suited for applications which require a high SNR and a wide dynamic range, as well as a relatively narrow bandwidth.

When the NSR is enabled, the noise level in a selected portion of the frequency band is reduced to a level below that of a conventional 12-bit ADC, while the noise level outside of this band is significantly higher. The SNR achievable in this mode is about 78 dBFS when integrated across 50% of the Nyquist bandwidth. This is an optimum selection for applications where the full Nyquist bandwidth of the ADC is not needed and where the digital signal post-processing of the ADC data is capable of removing the out-of-band noise added by the NSR.

Figures 3-26 and 3-29 show the SNR/SFDR versus input amplitude with NSR enabled.

4.5.4 DECOUPLING CIRCUITS FOR INTERNAL VOLTAGE REFERENCE AND BANDGAP OUTPUT

The device has two internal voltage references: REF0 and REF1. REF0 is the internal voltage reference for the ADC input stage, while REF1 is for all remaining stages. These internal references require external capacitors for stable operation. These capacitors are embedded in the TFBGA-121 package. In the VTLA-124 package, the user must provide these external capacitors on the PCB at the REF1+/REF1- and REF0+/REF0- pins.

Figure 4-7 shows the recommended circuit for the REF1 and REF0 pins for the VTLA-124 package. Three parallel capacitors are recommended between the positive and negative reference pins. The negative reference pin is then grounded through a 220 nF capacitor. The values for the parallel capacitors are 22 nF, 220 nF and 2.2 µF. The capacitors should be placed as close to the ADC as possible with short and thick traces. Vias on the PCB are not recommended for this reference pin circuit.

The internal bandgap voltage output, which is a part of the reference circuit, is also available at the V_{BG} pin. This pin needs an external decoupling capacitor (2.2 µF) for the VTLA-124 package, as shown in Figure 4-7. In the TFBGA-121 package, the decoupling capacitor is also embedded the same as the reference. Therefore, this circuit is not required.

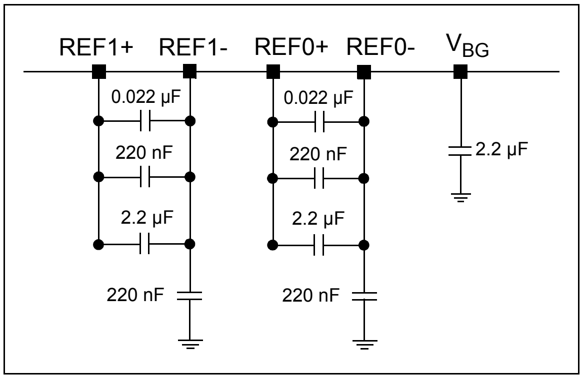


FIGURE 4-7: *External Circuit for Voltage Reference and V_{BG} pins for the VTLA-124 Package. Note that this external circuit is not required for the TFBGA-121 package.*

4.6 External Clock Input

For optimum performance, the MCP37XXX requires a low jitter differential clock input at the CLK+ and CLK− pins. Figure 4-8 shows the equivalent clock input circuit.

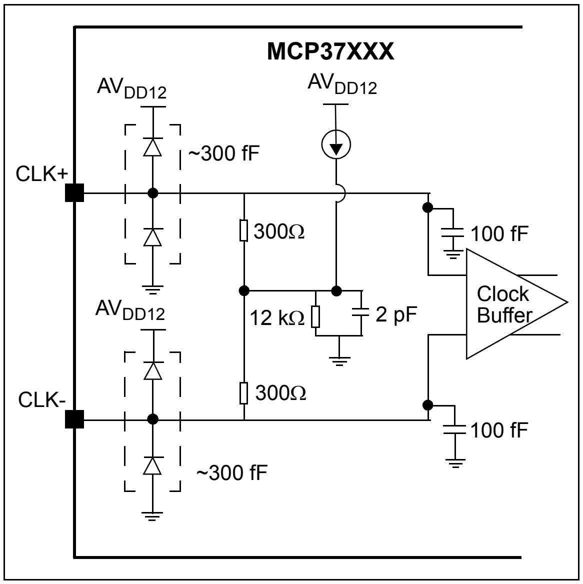


FIGURE 4-8: *Equivalent Clock Input Circuit.*

The clock input amplitude range is between 300 mV$_{P-P}$ and 800 mV$_{P-P}$. When a single-ended clock source is used, an RF transformer or balun can be used to convert the clock into a differential signal for the best ADC performance. Figure 4-9 shows an example clock input circuit. The common-mode voltage is internally generated and a center-tap is not required. The back-to-back Schottky diodes across the transformer secondary limit the clock amplitude to approximately 0.8 V_{P-P} differential. This limiter helps prevent large voltage swings of the clock while preserving the high slew rate that is critical for low jitter.

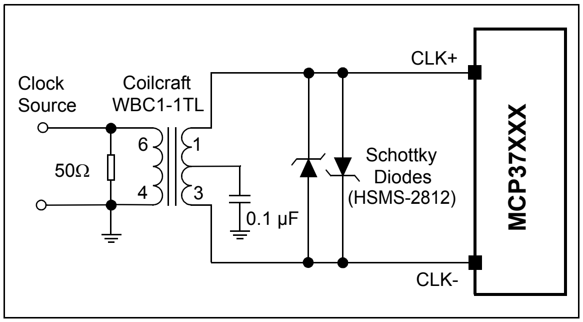


FIGURE 4-9: *Transformer-Coupled Differential Clock Input Configuration.*

4.6.1 CLOCK JITTER AND SNR PERFORMANCE

In a high speed-pipelined ADC, the SNR performance is directly limited by linearity, thermal noise and clock jitter. Thermal noise is independent of input clock and dominant at low input frequency. On the other hand, the clock jitter becomes a dominant term as input frequency increases. Equation 4-2 shows the SNR jitter component, which is expressed in terms of the input frequency (f_{IN}) and the total amount of clock jitter (T_{Jitter}), where T_{Jitter} is a sum of two components:

- Input clock jitter (phase noise)
- Internal aperture jitter (due to noise of the clock input buffer)

EQUATION 4-2: SNR VS. CLOCK JITTER

$$SNR_{Jitter}(dBc) = -20 \times \log_{10}(2\pi \times f_{IN} \times T_{Jitter})$$

where the total jitter term (T_{Jitter}) is given by:

$$T_{Jitter} = \sqrt{(t_{Jitter,\ Clock\ Input})^2 + (t_{Aperture,\ ADC})^2}$$

The clock jitter and aperture jitter are not statistically correlated to each other. The clock jitter can be minimized by using a high-quality clock source and jitter cleaners, as well as a band-pass filter at the external clock input, while a faster clock slew rate improves the ADC aperture jitter.

With a fixed amount of clock jitter, the SNR degrades as the input frequency increases. This is illustrated in Figure 4-10. If the input frequency increases from 10 MHz to 20 MHz, the maximum achievable SNR degrades about 6 dB. For every decade (e.g., 10 MHz to 100 MHz), the maximum achievable SNR due to clock jitter is reduced by 20 dB.

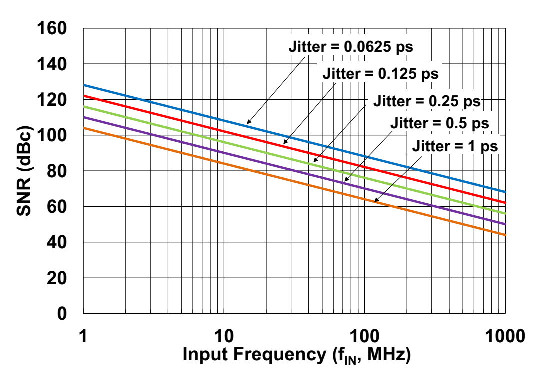


FIGURE 4-10: *SNR vs. Clock Jitter.*

4.6.2 CLOCK DUTY CYCLE

The ADC performance is sensitive to the clock duty cycle. The ADC achieves optimum performance with 50% duty cycle and all performance characteristics are ensured when the duty cycle is 50% with ±1% tolerance. This device has an internal clock duty cycle correction circuit, which can be enabled by using the EN_DUTY bit setting in Address 0x52 (Register 5-7). However, the duty cycle correction process adds additional jitter noise to the clock signal. Therefore, using this option is only recommended when an asymmetrical input clock source causes significant performance degradation or the input clock source is not stable. See more details of setting EN_DUTY in Address 0x52 (Register 5-7).

4.7 ADC Clock Selection and PLL Output Frequency Control

4.7.1 ADC CLOCK SELECTION

The user can select the ADC timing source (internal PLL or external clock) using the clock source selection bit setting. See CLK_SOURCE in Address 0x53 (Register 5-8).

4.7.1.1 External Clock for ADC Timing

When CLK_SOURCE = `0`, the external clock input (at CLK+ and CLK- pins) becomes the sampling frequency (f_S) of the ADC core and also the input frequency for the DLL circuit. See Figure 4-11 for details on the DLL block. The user can control the phase of the DLL output using DLL_PHDLY<2:0> in Address 0x52 (Register 5-7).

Note: The on-board phase lock loop (PLL) is not used for this setting.

4.7.1.2 Phase Lock Loop (PLL) Output for ADC Timing

When CLK_SOURCE = `1`, the PLL output frequency is used as the sampling frequency (f_S) of the ADC core. The recommended PLL output clock range is from 80 MHz to 250 MHz. The external clock input is used as the PLL reference frequency. The range of the clock input frequency is from 5 MHz to 250 MHz.

Note: The PLL mode is only supported for sampling frequencies greater than 80 Msps.

4.7.2 PLL OUTPUT FREQUENCY AND CONTROL PARAMETERS

The internal PLL can provide a stable timing output ranging from 80 MHz to 250 MHz. Figure 4-11 shows the charge-pump-based integer-N PLL and output control. The PLL includes various user control parameters for the desired output frequency. Table 4-4 summarizes the PLL control register bits and Table 4-5 shows an example of settings for the PLL charge pump and loop filter.

The PLL block consists of:

- Reference Frequency Divider (R)
- Prescaler – a feedback divider (N)
- Phase/Frequency Detector (PFD)
- Current Charge Pump
- Loop Filter – a 3rd order RC low-pass filter
- Voltage-Controlled Oscillator (VCO)

The final ADC core sampling frequency (f_S) is then obtained by dividing down the VCO output using PLL_OUTDIV<3:0>.

The external clock at the CLK+ and CLK- pins is the input frequency to the PLL. The range of input frequency (f_{REF}) is from 5 MHz to 250 MHz. This input frequency is divided by the reference frequency divider (R) which is controlled by the 10-bit wide PLL_REFDIV<9:0> setting. In the feedback loop, the VCO frequency is divided by the prescaler (N) using PLL_PRE<11:0>.

The final ADC core sampling frequency (f_S), ranging from 80 MHz to 250 MHz, is obtained after the output frequency divider (PLL_OUTDIV<3:0>). For stable operation, the user needs to configure the PLL with the following limits:

• Input clock frequency (f_{REF})	= 5 MHz to 250 MHz
• Maximum frequency at charge pump input (after PLL reference divider)	= 50 MHz
• VCO output frequency	= 1.075 to 1.325 GHz
• PLL output frequency after output divider	= 80 MHz to 250 MHz

The charge pump is controlled by the PFD and forces sink (DOWN) or source (UP) current pulses onto the loop filter. The charge pump bias current is controlled by the PLL_CHAGPUMP<3:0> bits, approximately 25 µA per step. The loop filter consists of a 3rd order passive RC filter. Table 4-5 shows the recommended settings of the charge pump and loop filter parameters, depending on the charge pump input frequency range (output of the reference frequency divider).

When the PLL is locked, it tracks the input frequency (f_{REF}) with the ratio of dividers (N/R). The PLL operating status is monitored by the PLL status indication bits: <PLL_VCOL_STAT> and <PLL_VCOH_STAT> in Address 0xD1 (Register 5-81).

Equation 4-3 shows the VCO output frequency (f_{VCO}) as a function of the two dividers and reference frequency.

EQUATION 4-3: VCO OUTPUT FREQUENCY

$$f_{VCO} = \left(\frac{N}{R}\right)f_{REF} = 1.075\ (GHz)\ to\ 1.325\ (GHz)$$

Where:

N = 1 to 4095 controlled by PLL_PRE<11:0>

R = 1 to 1023 controlled by PLL_REFDIV<9:0>

See Address 0x54 to 0x57 (Registers 5-9 to 5-12) for these bits settings.

The tuning range of the VCO is 1.075 GHz to 1.325 GHz. The N and R values must be chosen such that the VCO is within this range. In general, lower values of the VCO frequency (f_{VCO}) and higher values of the charge pump frequency (f_Q) should be chosen to optimize the clock jitter. Once the VCO output frequency is determined to be within this range, the user needs to set the final ADC sampling frequency (f_S) with the PLL output divider using PLL_OUTDIV<3:0>.

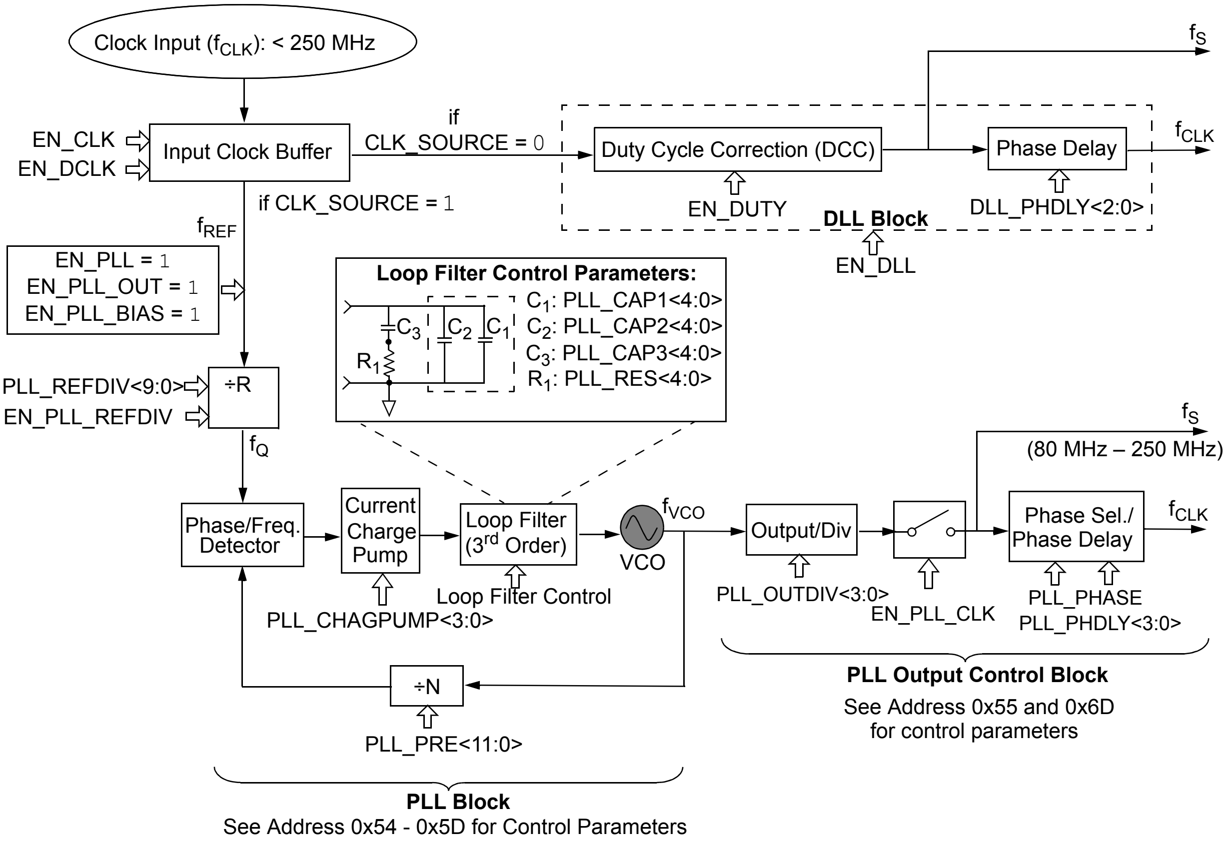
EQUATION 4-4: SAMPLING FREQUENCY

$$f_S = \left(\frac{f_{VCO}}{PLL\_OUTDIV}\right) = 80\ MHz\ to\ 250\ MHz$$

Table 4-6 shows an example of generating f_S = 200 MHz output using the PLL control parameters.

Note 1: In normal operation, the PLL maintains lock across all temperature ranges. It is not necessary to actively monitor the PLL unless extreme variations in the supply voltage are expected or the chip input frequency has been changed.

2: PLL recalibration is recommended when PLL control parameter settings are changed.



Note: VCO output range is 1.075 GHz – 1.325 GHz by setting PLL_REFDIV<10:0> and PLL_PRE<11:0>, with f_{REF} = 5 MHz – 200 MHz range.

$$f_{VCO} = \frac{N}{R} \times f_{REF} = (1.075 - 1.325)\ GHz$$

FIGURE 4-11: *PLL and DLL Control Blocks.*

TABLE 4-4: CONTROL PARAMETERS FOR PLL AND CLK

Control Parameter	Register	Descriptions
Clock Source Control		
CLK_SOURCE	0x53	Select internal timing source CLK_SOURCE = `1` selects the PLL output as the ADC clock source.
EN_DUTY	0x52	Enable duty cycle correction of the clock input when external clock input is selected as timing source (**Note 1**)
PLL Calibration and Status Indication Bits		
PLL_CALTRIG	0x6B	PLL circuit calibration (**Note 2**)
PLL_CAL_STAT	0xD1	PLL auto-calibration status indication
PLL_VCOL_STAT	0xD1	PLL drifts out-of-lock with low VCO frequency
PLL_VCOH_STAT	0xD1	PLL drifts out-of-lock with high VCO frequency
PLL Global Variable Setting Bits		
EN_PLL	0x59	Master enable bit for the PLL circuit
EN_PLL_OUT	0x5F	Master enable bit for the PLL output
EN_PLL_BIAS	0x5F	Master enable bit to enable the PLL bias
EN_PLL_REFDIV	0x59	Master enable bit for the PLL circuit. Enable PLL reference divider.
EN_PLL_CLK	0x6D	EN_PLL_CLK = `1` enable PLL output clock to the ADC circuits
PLL_PHDLY<3:0>	0x6D	Delay PLL Output up to 15 cycles of VCO clocks
PLL_PHASE	0x6D	Select PLL phase for delay line
PLL Block and PLL Output Control Settings		
PLL_REFDIV<9:0>	0x54-0x55	PLL Reference Divider (R) (see Table 4-6)
PLL_PRE<11:0>	0x56-0x57	PLL Prescaler (N) (see Table 4-6)
PLL_OUTDIV<3:0>	0x55	PLL Output Divider (see Table 4-6)
PLL_CHAGPUMP<3:0>	0x58	PLL charge pump bias current control: from 25 µA to 375 µA, 25 µA per step
PLL_RES<4:0>	0x5A	PLL loop filter resistor value selection (see Table 4-5)
PLL_CAP3<4:0>	0x5A	PLL loop filter capacitor 3 value selection (see Table 4-5)
PLL_CAP2<4:0>	0x5D	PLL loop filter capacitor 2 value selection (see Table 4-5)
PLL_CAP1<4:0>	0x5C	PLL loop filter capacitor 1 value selection (see Table 4-5)

Note 1: Duty cycle correction is not recommended when high quality external clock is used.

2: PLL recalibration is needed after reprogramming of the PLL block.

TABLE 4-5: RECOMMENDED PLL CHARGE PUMP AND LOOP FILTER PARAMETER VALUE SETTINGS EXAMPLE

PLL Charge Pump and Loop Filter Parameter (Note 1)	$f_Q = f_{REF}$/PLL_REFDIV		
	$5\text{ MHz} > f_Q$	$5\text{ MHz} \leq f_Q < 25\text{ MHz}$	$25\text{ MHz} \leq f_Q$
PLL_CHAGPUMP<3:0>	0x04	0x04	0x04
PLL_RES<4:0>	0x1F	0x1F	0x07
PLL_CAP3<4:0>	0x07	0x02	0x07
PLL_CAP2<4:0>	0x07	0x01	0x08
PLL_CAP1<4:0>	0x07	0x01	0x08

Note 1: See Table 4-4 for the parameter details.

TABLE 4-6: EXAMPLE PLL CONTROL PARAMETERS FOR GENERATING f_S = 200 MHz WITH f_{REF} = 100 MHz

PLL Control Parameter	Value	Descriptions
f_{REF}	100 MHz	f_{REF} is coming from the external clock input
Target f_{VCO}	1.2 GHz	Range of f_{VCO} = 1.0375 GHz – 1.325 GHz
Target f_S	200 MHz	ADC sampling frequency (Note 2)
Target f_Q	10 MHz	$f_Q = f_{REF}$/PLL_REFDIV (see Table 4-5)
PLL Reference Divider (R)	10	PLL_REFDIV<9:0> = 0x0A (Note 1)
PLL Prescaler (N)	120	PLL_PRE<11:0> = 0x78 (Note 1)
PLL Output Divider	6	PLL_OUTDIV<3:0> = 0x06 (Note 2)

Note 1: $f_{VCO} = (N/R) \times f_{REF} = (12) \times 100\text{ MHz} = 1.2\text{ GHz}$

2: $f_S = f_{VCO}/\text{PLL\_OUTDIV} = 1.2\text{ GHz}/6 = 200\text{ MHz}$

4.8 Digital Signal Post-Processing (DSPP) Options

While the device converts the analog input signals to digital output codes, the user can enable various digital signal post-processing options for special applications.

These options are individually enabled or disabled by setting the configuration bits. Table 4-7 summarizes the digital signal post-processing (DSPP) options that are available for each device family.

TABLE 4-7: DIGITAL SIGNAL POST-PROCESSING (DSPP) OPTIONS

Digital Signal Post-Processing Option	Available Operating Mode	Offering Device
Fractional Delay Recovery (FDR)	Dual and octal-channel modes	MCP37211-200 MCP37D11-200
FIR Decimation Filters	Single and dual-channel modes CW octal-channel mode DDC for I and Q data	
Noise-Shaping Requantizer (NSR)	Single and dual-channel modes	
Digital Gain and Offset Correction per Channel	Available for all channels	
Digital-Down Conversion (DDC)	Single and dual-channel modes CW octal-channel mode	MCP37D11-200
Continuous Wave (CW) Beamforming	CW octal-channel mode	

4.8.1 FRACTIONAL DELAY RECOVERY FOR DUAL AND OCTAL-CHANNEL MODES

When the device is used in multi-channel mode, it samples the channel inputs sequentially using a MUX, while the ADC core is operating at a constant full speed. This sequential sampling of multiple channels introduces a time delay between the sampling of different input channels relative to a multi-core ADC which would sample all inputs at the same instant. The fractional delay recovery (FDR) option digitally compensates the time delay of the sampling events.

This FDR feature is available in dual and octal-channel modes only. When the FDR is enabled, a high-order, band-limited interpolation filter deskews the sampling instant within a limited input bandwidth and synthetically removes the time delay of the input sampling. Figure 4-12 shows the simplified block diagram for the ADC output data path with FDR. The related configuration register bits are listed in Table 4-8.

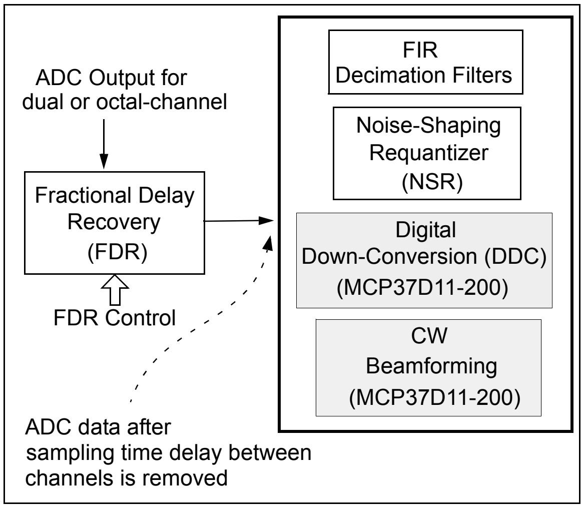


FIGURE 4-12: *Simplified Block Diagram for ADC Output Data Path with Fractional Delay Recovery Option. Note that Fractional Delay Recovery occurs prior to other DSPP features.*

TABLE 4-8: CONTROL PARAMETERS FOR FRACTIONAL DELAY RECOVERY (FDR)

Channel Operation	Control Parameter	Register	Descriptions
Global Control for Both Dual and Octal-Channel Modes	EN_FDR	0x79	Enable FDR features
	FDR_BAND	0x81	Select 1st or 2nd Nyquist band
Dual-Channel	SEL_FDR = `0`	0x81	Select FDR for Dual-Channel mode
	SEL_DPP = `0`	0x81	Select Digital Post-Processing (DPP) feature for Dual-Channel mode
	EN_DPPDUAL	0x79	Enable all digital post-processing functions for Dual-Channel operation
Octal-Channel	SEL_FDR = `1`	0x81	Select FDR for Octal-Channel mode
	SEL_DPP = `1`	0x81	Select Digital Post-Processing (DPP) feature for Octal-Channel mode

Table 4-9 shows the input bandwidth limits of the FDR feature for distortion less than 0.1 mdB (0.1 × 10^{-3} dB), where f_S is the sampling frequency per channel. Figures 4-13 and 4-14 show the responses of the dual-channel and octal-channel FDRs, respectively.

TABLE 4-9: INPUT BANDWIDTH REQUIREMENT FOR FDR

Bandwidth in percentage of f_S[1]	Nyquist Band
Dual-Channel Mode	
0 – 45%	1st Nyquist Band
55 – 100%	2nd Nyquist Band
45 – 55%	Avoid
Octal-Channel Mode	
0 – 38%	1st Nyquist Band

Note 1: f_S is the sampling frequency per channel. Distortion is less than 0.1 mdB.

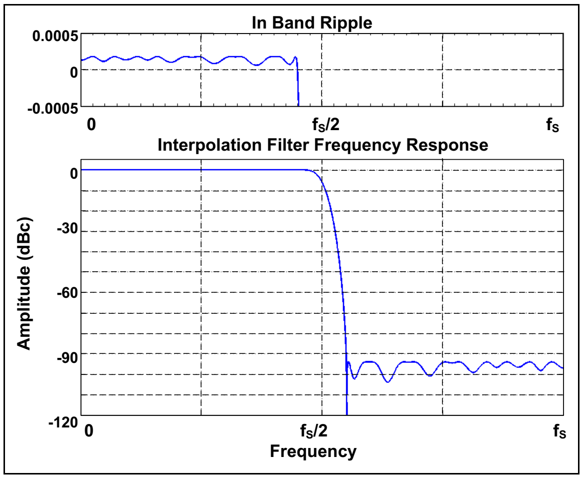


FIGURE 4-13: Response of the Dual-Channel Fractional Delay Recovery. f_S is the sampling frequency.

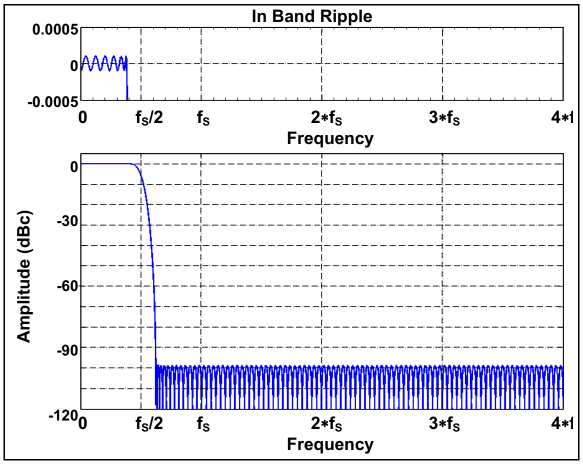


FIGURE 4-14: Response of the Octal-Channel Fractional Delay Recovery. f_S is the sampling frequency.

4.8.2 NOISE-SHAPING REQUANTIZER (NSR)

The device includes 11-bit and 12-bit digital Noise-Shaping Requantizer (NSR) options. When this function is enabled (see Register 5-35), the output data are requantized to 11-bit or 12-bit, respectively. The NSR reshapes the requantization noise function, which pushes most of the noise outside the frequency band of interest. As a result, the noise floor within the selected bandwidth is substantially lower than that of a typical 12-bit ADC.

To ensure the stability of the NSR, the input signal to the NSR should be limited to less than -0.8 dBFS (~90% of f_S). This can be achieved either by limiting the analog input level or by adjusting the digital gain control. See **Section 4.9 "Digital Offset and Digital Gain Settings"** and Registers 5-63 to 5-70 for details on the digital gain control. Input levels higher than -0.8 dBFS may corrupt the NSR output and should be avoided.

The NSR feature is available only for the single and dual-channel modes and can be independently controlled per channel via the register settings. Two NSRs are used:

- NSRA for channel A
- NSRB for channel B

In single-channel mode, only NSRA is used. In dual-channel mode, both NSRA and NSRB are used: NSRA for the first selected channel and NSRB for the second selected channel. Both have 11-bit and 12-bit options. Each NSR block consists of a series of filters, which are selectable using the NSRA<6:0> and NSRB<6:0> register bit settings. Each filter is defined by a specific percentage bandwidth and center frequency. The available percentage bandwidths are:

- 11-bit mode: 22% and 25% of the sampling frequency
- 12-bit mode: 25% and 29% of the sampling frequency

The center frequency of the band is tunable such that the frequency band of interest can be placed anywhere within the Nyquist band. Table 4-10 lists all NSR-related registers. Equations 4-5 and 4-6 describe the NSR bandwidth of the 11-bit and 12-bit option, respectively.

EQUATION 4-5: NSR BANDWIDTH FOR 11-BIT OPTION

(a) 22% BW:

$$\frac{f_{Center}}{f_S} = 0.12 + \frac{0.26}{20} \times NSR$$

where 0 ≤ NSR ≤ 20

(b) 25% BW:

$$\frac{f_{Center}}{f_S} = 0.125 + \frac{0.25}{20} \times (NSR - 21)$$

where 21 ≤ NSR ≤ 41

where NSR is the NSR filter number. See Tables 4-11 and 4-12 for details.

EQUATION 4-6: NSR BANDWIDTH FOR 12-BIT OPTION

(a) 22% BW:

$$\frac{f_{Center}}{f_S} = 0.125 + \frac{0.25}{20} \times (NSR - 42)$$

where 42 ≤ NSR ≤ 62

(b) 29% BW:

$$\frac{f_{Center}}{f_S} = 0.15 + \frac{0.2}{12} \times (NSR - 63)$$

where 63 ≤ NSR ≤ 76

where NSR is the NSR filter number. See Tables 4-11 and 4-12 for details.

The center frequency of the band is tuned such that the frequency spectrum of interest can be placed anywhere within the Nyquist band. Figure 4-15 shows a graphical demonstration of the NSR bandwidth, which is a percentage of the ADC sampling frequency.

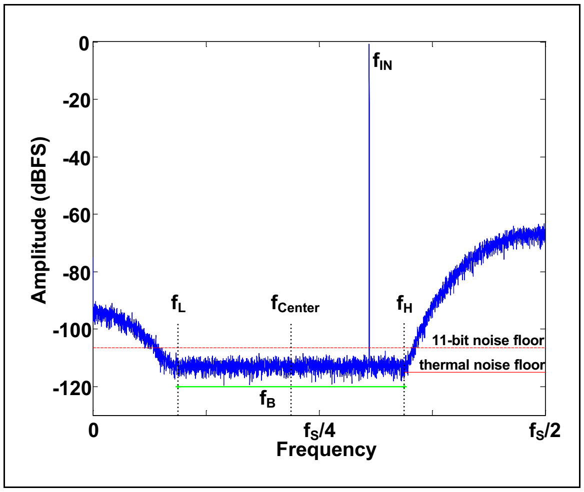


FIGURE 4-15: *Graphical demonstration of the NSR filter's transfer function. Note that f_B is controlled as a percentage of the sampling frequency (f_S).*

Tables 4-11 and 4-12 show the NSR filter selections. The selectable filters (tuning word) for each mode are:

- 11-bit mode: 0 to 41
- 12-bit mode: 42 to 76

NSR does not affect harmonic distortion. Various FFT spectrum plots when NSR is applied are shown in Figures 3-14 to 3-15, Figures 3-17 to 3-20 and Figures 3-22 to 3-23. SNR and SFDR performance versus input amplitude when NSR is enabled is shown in Figures 3-26 and 3-29. In this case, SNR and SFDR are measured within the 12-bit mode NSR bandwidth (25% of the sampling frequency). When the NSR block is disabled, the ADC data is provided directly to the output.

TABLE 4-10: REGISTER CONTROL PARAMETERS FOR NSR

Control Parameter	Register	Descriptions
NSR Enable bits		
<EN_NSRA_11>	0x7A	Enable 11-bit NSR for channel A
<EN_NSRA_12>	0x7A	Enable 12-bit NSR for channel A
<EN_NSRB_11>	0x7A	Enable 11-bit NSR for channel B
<EN_NSRB_12>	0x7A	Enable 12-bit NSR for channel B
NSR Settings		
NSRA<6:0>	0x78	NSR A settings for single-channel or channel A for dual-channel mode
NSRB<6:0>	0x79	NSR B settings for channel B in dual-channel mode
NSR Block Reset Control		
<EN_NSR_RESET>	0x78	Resets NSR in the event of overload
Digital Post Processing (DPP) Function Block Settings		
EN_DPPDUAL	0x79	Enable DPP block for dual-channel mode

TABLE 4-11: 11-BIT NSR FILTER SELECTION

NSR Filter No. (Tuning Word)	f_{Center}/f_S (Note 1)	f_B (% of f_S)	NSRA<6:0> NSRB<6:0>
0	0.15	22	000-0000
1	0.16	22	000-0001
2	0.17	22	000-0010

19	0.34	22	001-0011
20	0.35	22	001-0100
21	0.15	25	001-0101
22	0.16	25	001-0110
23	0.17	25	001-0111

40	0.34	25	010-1000
41	0.35	25	010-1001

Note 1: Increment step size per f_{Center}/f_S:
a) 0.01 from Filter 0 to Filter 20
b) 0.01 from Filter 21 to Filter 41

2: Filters 0 - 41 are used for 11-bit mode only. If these are used for 12-bit mode, the output becomes unknown state.

TABLE 4-12: 12-BIT NSR FILTER SELECTION

NSR Filter No. (Tuning Word)	f_{Center}/f_S (Note 1)	f_B (% of f_S)	NSRA<6:0> NSRB<6:0>
42	0.15	25	010-1010
43	0.16	25	010-1011
44	0.17	25	010-1100

61	0.34	25	011-1101
62	0.35	25	011-1110
63	0.19	29	011-1111
64	0.2	29	100-0000
65	0.21	29	100-0001

75	0.31	29	100-1011
76	0.32	29	100-1100

Note 1: Increment step size per f_{Center}/f_S:
a) 0.01 from Filter 42 to Filter 62
b) 0.01 from Filter 63 to Filter 76

2: Filters 0 - 41 are used for 11-bit mode only. If these are used for 12-bit mode, the output becomes unknown state.

4.8.3 DECIMATION FILTERS

The decimation feature is available in single and dual-channel modes. Figure 4-16 shows a simplified decimation filter block and Table 4-14 shows the register settings. The decimation rate is controlled by FIR_A<8:0> and FIR_B<7:0> settings in Addresses 0x7A – 0x7C (Registers 5-35 to 5-37). These registers are thermometer-encoded.

In single-channel mode, FIR B is disabled and only FIR A is used. In this mode, the maximum programmable decimation rate is 512x using nine cascaded decimation stages.

In dual-channel mode or when using the Digital Down-Conversion (DDC) in I/Q mode, both FIR A and FIR B are used (see Figure 4-16). In this case, both channels are set to the same decimation rate. Note that stage 1A in FIR A is unused: the user must clear FIR_A<0> in Address 0x7A (Register 5-35). In dual-channel mode, the maximum programmable decimation rate is up to 256x, which is ½ of the single channel decimation rate (512x).

The overall SNR performance can be improved with higher decimation rate up to 16x, but limited to about 73.7 dBFS after 16x. This limitation is mainly due to the relative quantization noise level with respect to the 12-bit LSB size. Decimation rates beyond 16x do not further improve SNR but do serve to filter the output data and reduce the overall output data rate. Table 4-13 summarizes decimation rate versus SNR.

When decimation is used, it also reduces the output clock rate and the output bandwidth by a factor equal to the decimation rate applied: the output clock rate is therefore no longer equal to the ADC sampling clock. The user needs to adjust the output clock and data rates in Address 0x02 (Register 5-3) based on the decimation applied. The DLL should also be disabled in this mode. This allows the output data to be synchronized to the output data clock.

Phase shifts in the output clock can be achieved using DCLK_PHDLY_DEC<2:0> in Address 0x64 (Register 5-22). When decimation of 2x is used, only four output sampling phases are available, while all eight clock phases are available for other decimation rates. Table 4-14 summarizes the related control parameters for using decimation filters.

4.8.3.1 Using Decimation with CW Beamforming and Digital Down-Conversion

Decimation can be used in conjunction with CW octal-channel mode or DDC. In CW octal-channel mode operation, the eight-input channels are summed into a single channel prior to entering the decimation filters. When DDC is enabled, the I and Q outputs can be decimated using the same signal path for the dual-channel mode: I and Q data are fed into Channel A and B, respectively.

In DDC mode, the half-band filter already includes a 2x decimation. Therefore, the maximum decimation rate setting for I/Q filtering is 128x for the FIR_A<8:1> and FIR_B<7:0>. See **Section 4.8.4 "Digital Down-Conversion (MCP37D11-200 Only)"** for details.

Note: Fractional Delay Recovery, Digital Gain/Offset adjustment and DDC for I/Q data options occur prior to the decimation filters if they are enabled.

TABLE 4-13: DECIMATION RATE VS. SNR PERFORMANCE

Decimation Rate	SNR (dBFS)
2x	71.4
4x	72.2
8x	72.9
16x	73.3
32x	73.7
64x	
128x	
256x	
512x	

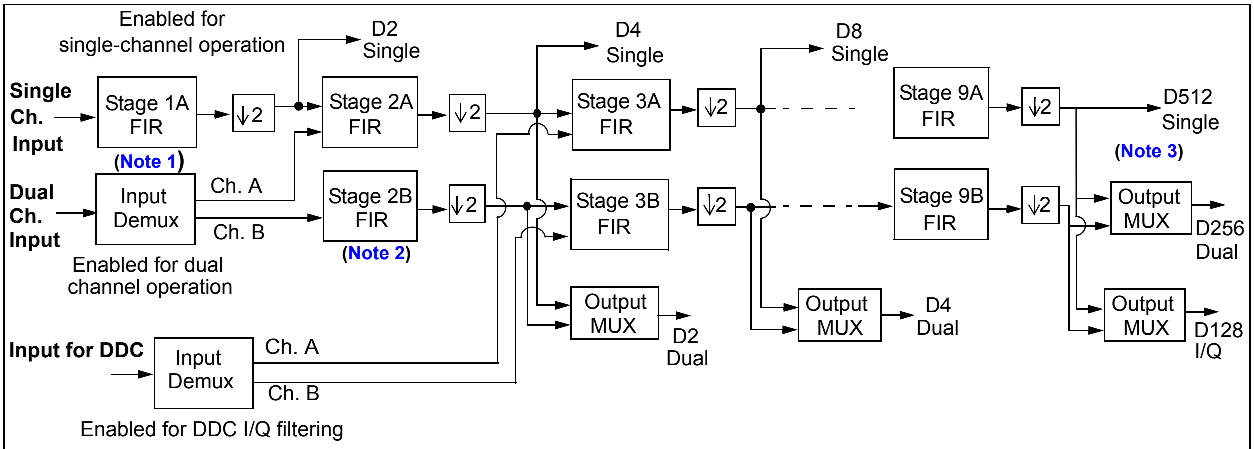
Note: The above data is validated with f_S = 200 Msps, f_{IN} = 5 MHz, A_{IN} = -1 dBFS.

TABLE 4-14: REGISTER CONTROL PARAMETERS FOR USING DECIMATION FILTERS

Control Parameter	Register	Descriptions
Decimation Filter Settings		
FIR_A<8:0>	0x7A, 0x7B	Channel A FIR configuration for single or dual-channel mode
FIR_B<7:0>	0x7C	Channel B FIR configuration for single or dual-channel mode
Output Data Rate and Clock Rate Settings (Note 1)		
OUT_DATARATE<3:0>	0x02	Output data rate: equal to decimation rate
OUT_CLKRATE<3:0>	0x02	Output clock rate: equal to decimation rate
Output Clock Phase Control Settings (Note 2)		
EN_PHDLY_DEC	0x64	Enable digital output phase delay when decimation filter is used
DCLK_PHDLY_DEC<2:0>	0x64	Digital output clock phase delay control
Digital Signal Post-Processing (DSPP) Function Block Settings		
EN_DSPPDUAL	0x79	Enable dual-channel decimation

Note 1: The output data and clock rates must be updated when decimation rates are changed.

2: Output clock (DCLK) phase control is used when the output clock is divided by OUT_CLKRATE<3:0> bit settings.



Note 1: Stage 1A FIR is the first stage of FIR A filter. Used in single-channel mode only and must be by-passed in dual-channel mode by setting FIR_A<0> = 0 in Address 0x7A (Register 5-35).

2: (a) Single-channel mode: Only Channel A is used and controlled by the FIR_A<8:0>.
(b) Dual-channel mode or I/Q filtering in DDC mode: Both Channel A and Channel B are used (Channel A for the first channel or I data and Channel B for the second channel or Q data).

3: Maximum decimation rate:
(a) When I/Q filtering in DDC mode is not used: 512x for single-channel and 256x for dual-channel mode.
(b) I/Q filtering in DDC mode: 128x each for FIR_A<8:1> and FIR_B<7:0>.

FIGURE 4-16: *Simplified Block Diagram of Decimation Filters.*

4.8.4 DIGITAL DOWN-CONVERSION (MCP37D11-200 ONLY)

The Digital Down-Conversion (DDC) feature is available in single, dual and CW octal-channel modes in MCP37D11-200. This feature can be optionally combined with the decimation filter and used to:

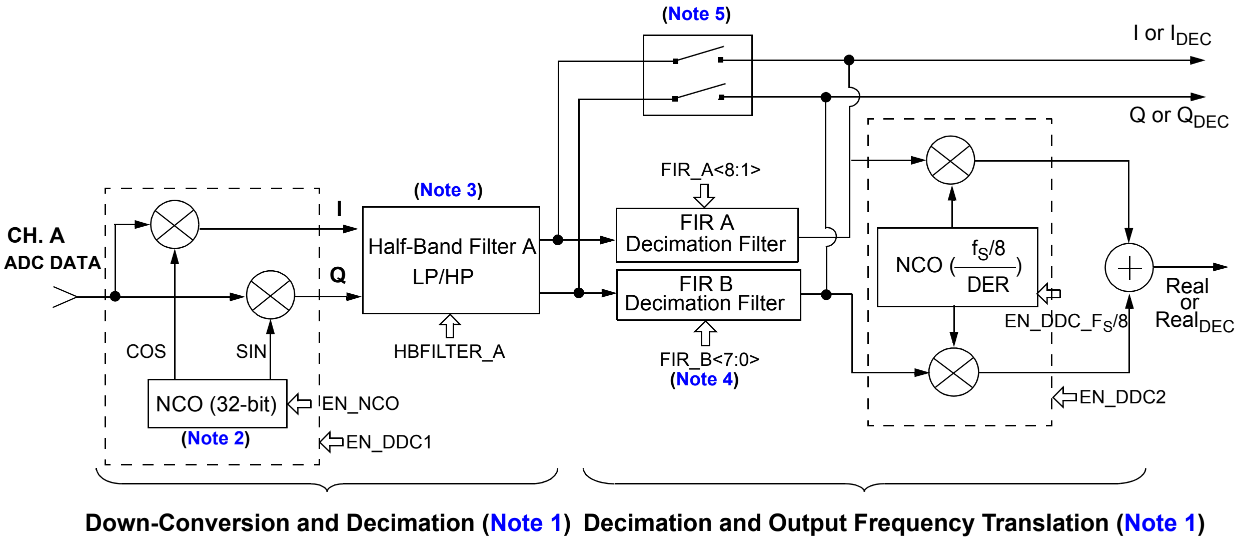
- translate a portion of the input frequency spectrum to lower frequencies
- remove the unwanted out-of-band portion
- output the resulting signal as either I/Q data or a real signal centered at ¼ of the output data rate

For example, if the ADC is sampling a single-channel input at 200 Msps, but the user is only interested in a 5 MHz span which is centered at 67 MHz, digital down-conversion may be used to mix the sampled ADC data with 67 MHz to convert it to DC. The resulting signal can then be decimated by 16x such that the bandwidth of the ADC output is 6.25 MHz (200 Msps/16x decimation gives 12.5 Msps with 6.25 MHz Nyquist bandwidth). If $f_S/8$ mode is selected, then a single 25 Msps channel is output, where 6.25 MHz in the output data corresponds to 67 MHz at the ADC input. If I/Q mode is selected, then two 12.5 Msps channels are output, where DC corresponds to 67 MHz and the channels represent In-Phase and Quadrature components of the down-conversion. Figures 4-17 and 4-18 show the DDC block diagrams of single and dual-channels, respectively. Figures 4-19 and 4-20 show the half-band filter responses.

This DDC feature can be used in a variety of high-speed signal-processing applications, including digital radio, wireless base stations, radar, cable modems, digital video, etc. Since the processing is achieved completely in the digital domain, the result is not affected by classical nonlinearities typical in analog implementations.

4.8.4.1 Single-Channel DDC

Figure 4-17 shows the single-channel DDC configuration. The DDC includes a 32-bit numerically controlled oscillator (NCO), a selectable (high/low) half-band filter, optional decimation and two output modes (I/Q or $f_S/8$). Phase and amplitude dither may be enabled for the NCO with a negligible performance penalty. Each of these processing sub-blocks are individually controlled. Examples of setting registers for selected output type are shown in Tables 4-15 and 4-16 in **Section 4.8.5 “Examples of Register Settings for Using Decimation and DDC”**.

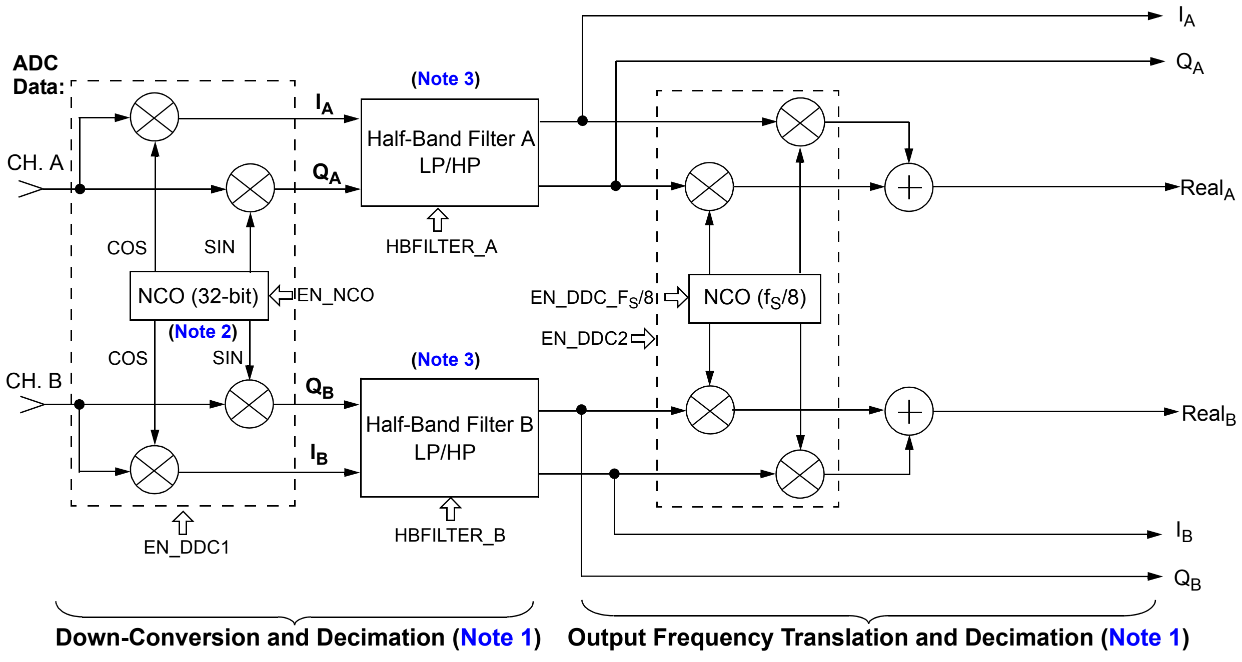


Note 1: See Address 0x80 - 0x81 (Registers 5-41 – 5-42) for the control parameters.
2: See Figure 4-21 for details of NCO control block.
3: Half-band Filter A includes a single-stage decimation filter.
4: See Figure 4-16 for details.
5: Switches are closed if decimation filter is not used and open if decimation filter is used.

FIGURE 4-17: *Simplified DDC Block Diagram for Single-Channel Mode. See Tables 4-15 and 4-16 for Using this DDC Block.*

4.8.4.2 Dual-Channel DDC

Figure 4-18 shows the dual-channel DDC configuration. Each channel includes the same processing elements as shown in the single-channel DDC, however the I/Q outputs cannot be separately decimated since the device only supports two channels of decimation (four would be required for I/Q of Channel A and I/Q of Channel B). The decimation option can be used if the DDC output after the half-band filter is up-converted by $f_S/8$ for each channel. Otherwise, I/Q of each channel will be output separately similar to a four-channel input device with the WCK output pin toggling synchronously with the I-data of Channel A. Note that the NCO phase can be adjusted uniquely for each of the two input channels (see Figure 4-21). Examples of setting registers for selected output type are shown in Tables 4-17 and 4-18.



Note 1: See Address 0x80 – 0x81 for the control parameters.
2: See Figure 4-21 for details of NCO control block.
3: Half-band filter A and B include a single-stage decimation filter.

FIGURE 4-18: *Simplified DDC Block Diagram for Dual-Channel Mode. See Tables 4-17 and 4-18 for Using this DDC Block.*

4.8.4.3 Half-Band Filter

The half-band digital filter is used to reduce the sample rate by a factor of 2 while rejecting aliases that fall into the band of interest. This filter is designed to operate as either a high-pass filter (Figure 4-19) or a low-pass filter (Figure 4-20) and to provide greater than 90 dB of attenuation for 20% (attenuation band) of the input sampling rate and less than 1 mdB (10^{-3} dB) of ripple for 20% (passband region) of the input sampling rate. For example, for an ADC sample rate of 200 Msps, this provides less than 1 mdB of ripple over a bandwidth of 40 MHz. The half-band filter is configured using the HBFILTER_A and HBFILTER_B parameters in Address 0x80 (Register 5-41). The filter responses of the half-band filter shown in Figures 4-19 and 4-20 indicate a ripple of 0.5 mdB and an alias rejection of 90 dB. The output of the half-band filter is a DC-centered complex signal (I and Q). This I and Q signal is then carried to the next down-conversion stage (DDC2) for frequency translation (up-conversion), if the DDC is enabled.

Note:	The half-band filter delays the data output by 80 clock cycles: 2 (due to decimation) x 40 cycles (due to propagations)

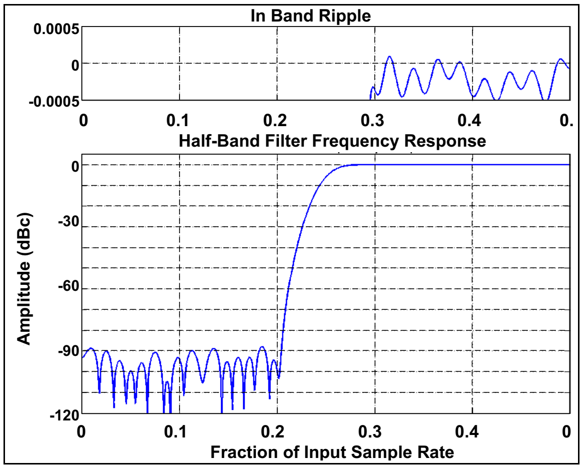


FIGURE 4-19: *High-Pass (HP) Response of Half-Band Filter.*

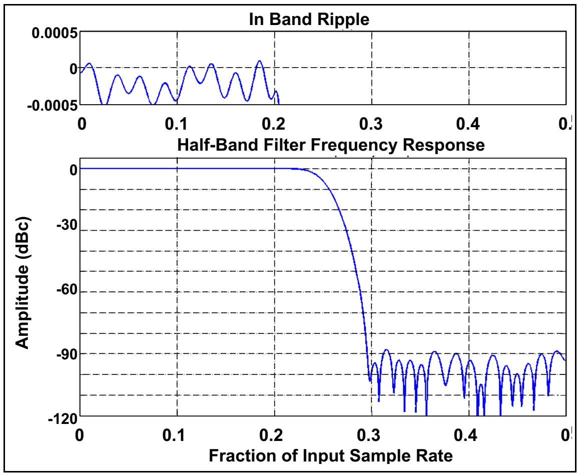


FIGURE 4-20: *Low-Pass (LP) Response of Half-Band Filter.*

4.8.4.4 Numerically Controlled Oscillator (NCO)

The on-board Numerically Controlled Oscillator (NCO) provides the frequency reference for the In-Phase and Quadrature mixers in the digital down-converter (DDC). Figure 4-21 shows the control signals associated with the NCO. In octal or dual-channel mode, the NCO allows the output phase to be adjusted on a per-channel basis.

> **Note:** The NCO is only used for DDC or CW octal-channel mode. It should be disabled when not in use.

The NCO frequency is programmed using the 32-bit wide unsigned register variable NCO_TUNE<31:0> in Addresses 0x82 – 0x85 (Registers 5-43 – 5-46). The following equation is used to setup the NCO_TUNE<31:0> setting:

EQUATION 4-7: NCO FREQUENCY

$$NCO\_TUNE<31:0> = round\left(2^{32} \times \frac{Mod(f_{NCO}, f_S)}{f_S}\right)$$

Where:

f_S = sampling frequency (Hz)
f_{NCO} = desired NCO frequency (Hz)
Mod (f_{NCO}, f_S) = gives the remainder of f_{NCO}/f_S

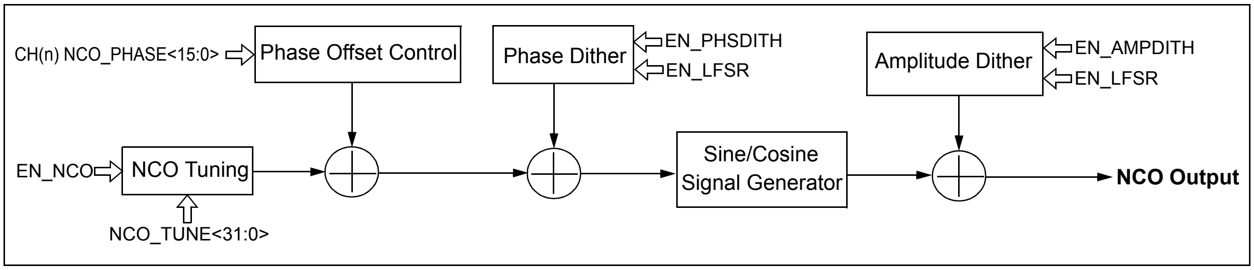


FIGURE 4-21: *NCO Block Diagram.*

4.8.4.5 NCO Amplitude and Phase Dither

The EN_AMPDITH and EN_PHSDITH parameters in Address 0x80 (Register 5-41) can be used for amplitude and phase dithering, respectively. In principle, these will dither the quantization error created by the use of digital circuits in the mixer and local oscillator, thus reducing spurs at the expense of noise. In practice, the DDC circuitry has been designed with sufficient noise and spurious performance for most applications. In the worst case scenario, the NCO has an SFDR of greater than 116 dB when the amplitude dither is enabled and 112 dB when disabled. Although the SNR (~93 dB) of the DDC is not significantly affected by the dithering option, using the NCO with dithering options enabled is always recommended for the best performance.

4.8.4.6 NCO for $f_S/8$ and $f_S/(8xDER)$

The output of the first down-conversion block (DDC1) is a complex signal (comprising I and Q data) which can then be optionally decimated further up to 64x to provide both a lower output data rate and input channel filtering. If $f_S/8$ mode is enabled, a second mixer stage (DDC2) will convert the I/Q signals to a real signal centered at half of the current Nyquist frequency; i.e., if the output data rate in I/Q mode is 25 Msps per channel (12.5 MHz Nyquist band), then in $f_S/8$ mode the output data rate would be 50 Msps and the signal would be recentered around 12.5 MHz. In single-channel mode, this is done at the output of the decimation filters (if used). In dual-channel mode, this must be done prior to the decimation. When decimation is enabled, the I/Q outputs are up-converted by $f_S/(8xDER)$, where DER is the additional decimation rate added by the FIR decimation filters. This provides a decimated output signal centered at $f_S/8$ or $f_S/(8xDER)$ in the frequency domain.

4.8.4.7 NCO Phase Offset Control

The user can add phase offset to the NCO frequency using the NCO phase offset control registers (Addresses 0x86 to 0x95 – Registers 5-47 – 5-62). CH(n)_NCO_PHASE<15:0> is the 16-bit wide NCO phase offset control parameter for Channel *n*. A 0x0000 value in the register corresponds to no offset and a 0xFFFF corresponds to an offset of 359.995°. The phase offset can be controlled with 0.005° per step. The following equation is used to program the NCO phase offset register:

EQUATION 4-8: NCO PHASE OFFSET

$$CH(n)\_NCO\_PHASE<15:0> = 2^{16} \times \frac{Offset\ Value\ (\phi)}{360}$$

Where:

n = channel number

Offset Value (ϕ) = desired phase offset value in degrees

A decimal number is used for the binary contents of the CH(n)_NCO_PHASE<15:0>.

4.8.4.8 In-Phase and Quadrature Signals

When the first down-conversion is enabled, it produces In-phase (I) and Quadrature (Q) components given by:

EQUATION 4-9: I AND Q SIGNALS

$$I = ADC \times COS(2\pi f_{NCO} t + \phi) \quad \text{(a)}$$

$$Q = ADC \times SIN(2\pi f_{NCO} t + \phi) \quad \text{(b)}$$

where:

$$\phi = 360 \times \frac{CH(n)\_NCO\_PHASE<15:0>}{2^{16}} \quad \text{(c)}$$
$$= 0.005493164° \times CH(n)\_NCO\_PHASE<15:0>$$

where:

ADC = output of the ADC block

ϕ = NCO phase offset of selected channel which is defined by the CH(n)_NCO_PHASE<15:0> in Address 0x86 - 0x95

t = k/f_S, with k =1, 2, 3,..., n

f_{NCO} = NCO frequency

I and Q data are output in an interleaved fashion where I data is output on the rising edge of the WCK. If I and Q output are selected in dual-channel mode with DDC enabled, I data of Channel 0 is output at the rising edge of WCK, followed by Q data of Channel 0, then I and Q data of Channel 1.

4.8.5 EXAMPLES OF REGISTER SETTINGS FOR USING DECIMATION AND DDC

The following tables show examples of setting registers for using decimation and digital down-conversion (DDC) depending on the output type selection. This feature is available in the MCP37D11-200 device only.

TABLE 4-15: REGISTER SETTINGS FOR DECIMATION AND DDC OPTIONS FOR SINGLE-CHANNEL MODE – EXAMPLE

Decimation Rate (by FIR A and FIR B) (Note 6)	DDC Mode	Addr. 0x02 (Note 1)	FIR A Filter		FIR B Filter	DDC1	DDC2	Dual-Channel DSPP Control	Output
			0x7A<6> (FIR_A<0>)	0x7B (FIR_A<8:1>)	0x7C (FIR_B<7:0>)	0x80<5,1,0> (Note 2)	0x81<6,3,2> (Note 3)	0x79<7> (EN_DSPPDUAL)	
0	Disabled	0x00	0	0x00	0x00	0,0,0	0,0,0	0	ADC
8	Disabled	0x33	1	0x03	0x00	0,0,0	0,0,0	0	ADC with decimation (÷8)
512	Disabled	0x99	1	0xFF	0x00	0,0,0	0,0,0	0	ADC with decimation (÷512)
0	I/Q	0x00 (Note 4)	0	0x00	0x00	1,0,1	0,0,0	0	I/Q Data
8	I/Q	0x33	0	0x07	0x07	1,0,1	0,0,0	0	Decimated I/Q (÷8)
0	f_S/8	0x11 (Note 5)	0	0x00	0x00	1,1,1	0,0,0	0	Real without using decimation filter (÷2)
8	f_S/8	0x44	0	0x07	0x07	1,0,1	1,0,0	0	Real with decimation (÷16)

Note 1: Output data and clock rate control register.

2: 0x80<5,1,0> = <EN_NCO, EN_DDC_FS/8, EN_DDC1>.

3: 0x81<6,3,2> = <EN_DDC, SEL_DSPP, 8CH_CW>.

4: Each of I/Q has 1/2 of f_S bandwidth. The combined bandwidth is the same as the f_S bandwidth. Therefore, the data rate adjustment is not needed.

5: Data rate is reduced by half since the Half-Band Filter A includes decimation of 2.

6: This decimation value is set using the decimation filter. When DDC is used, the actual total decimation is 2x larger since 2x is included from the DDC Half-Band Filter. Example: “single-channel, Decimation = 8x, DDC-IQ” option actually has 16x decimation with 8x provided by the decimation filter and 2x from the DDC Half-Band Filter.

TABLE 4-16: OUTPUT TYPE VS. CONTROL PARAMETERS FOR SINGLE-CHANNEL DDC – EXAMPLE

Output Type	Control Parameter	Register	Descriptions
Complex: I and Q	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 0	0x81	NCO(f_S/8/DER) is disabled
	EN_DDC2> = 0	0x80	DDC2 is disabled
	FIR_A<8:1> = 0x00	0x7B	FIR A decimation filter is disabled
	FIR_B<7:0> = 0x00	0x7C	FIR B decimation filter is disabled
	OUT_CLKRATE<3:0>	0x02	Output clock rate is not affected (no need to change)
Decimated I and Q: I_{DEC}, Q_{DEC}	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 0	0x81	NCO(f_S/8/DER) is disabled
	EN_DDC2 = 0	0x80	DDC2 is disabled
	FIR_A<8:1>	0x7B	Program FIR A filter for extra decimation (**Note 1**)
	FIR_B<7:0>	0x7C	Program FIR B filter for extra decimation (**Note 1**)
	OUT_CLKRATE<3:0>	0x02	Adjust the output clock rate to the decimation rate
Real: $Real_A$ after DDC (f_S/8/DER) without using Decimation Filter	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 1	0x81	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8 (**Note 3**)
	EN_DDC2 = 1	0x80	DDC2 is enabled
	FIR_A<8:1> = 0x00	0x7B	Decimation filter FIR A is disabled
	FIR_B<7:0> = 0x00	0x7C	Decimation filter FIR B is disabled
	OUT_CLKRATE<3:0> = 0001	0x02	Adjust the output clock rate to divided by 2 (**Note 2**)
Decimated Real: $Real_{A\_DEC}$ after Decimation Filter and DDC (f_S/8/DER)	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	EN_DDC_FS/8 = 1	0x81	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8/DER (**Note 3**).
	EN_DDC2 = 1	0x80	DDC2 is enabled
	FIR_A<8:1>	0x7B	Program FIR B filter for extra decimation (**Note 4**)
	FIR_B<7:0>	0x7C	Program FIR B filter for extra decimation (**Note 4**)
	OUT_CLKRATE<3:0>	0x02	Adjust the output clock rate to the total decimation rate including the 2x decimation by the Half-Band Filter A

Note 1: For I/Q decimation, the maximum decimation rate for the FIR A and FIR B is 128x each since the input is already decimated by 2x in the Half-Band Filter. See Figure 4-16 for details.

2: Divided by 2 is due to the 2x decimation included in the Half-Band Filter A.

3: DER is the decimation rate setting of FIR A and FIR B filters.

4: When this filter is used, the up-conversion frequency is reduced by the extra decimation rates (DER).

TABLE 4-17: REGISTER SETTINGS FOR DECIMATION AND DDC OPTIONS FOR DUAL-CHANNEL MODE – EXAMPLE

Decimation Rate (by FIR A and FIR B) (Note 7)	DDC Mode	Address 0x02 (Note 1)	FIR A Filter		FIR B Filter	DDC1	DDC2	Dual-Channel DSPP Control	Output
			0x7A<6> (FIR_A<0>)	0x7B (FIR_A<8:1>)	0x7C (FIR_B<7:0>)	0x80<5,1,0> (Note 2)	0x81<6,3,2> (Note 3)	0x79<7> (EN_DSPPDUAL)	
0	Disabled	0x00	0	0x00	0x00	0,0,0	0,0,0	0	ADC
8	Disabled	0x33	0	0x07	0x07	0,0,0	0,0,0	0	ADC with decimation (÷8)
256	Disabled	0x88	0	0xFF	0xFF	0,0,0	0,0,0	0	ADC with decimation (÷256)
0	I/Q	0x00 (Note 4)	0	0x00	0x00	1,0,1	0,0,0	1	I/Q data
0	$f_S/8$	0x11 (Note 5)	0	0x00	0x00	1,1,1	0,0,0	1	$Real_A/Real_B$ without using decimation filter (÷2)
8	$f_S/8$	0x44	0	0x0E	0x0E (Note 6)	1,1,1	0,0,0	1	Real with decimation filter (÷16)

Note 1: Output data and clock rate control register.
2: 0x80<5,1,0> = <EN_NCO, EN_DDC_FS/8, EN_DDC1>.
3: 0x81<6,3,2> = <EN_DDC, SEL_DSPP, 8CH_CW>.
4: Each of I/Q has 1/2 of f_S bandwidth. The combined bandwidth is the same as the f_S bandwidth. Therefore, the data rate adjustment is not needed.
5: Data rate is reduced by half since the Half-Band Filter A/B includes decimation of 2.
6: 0x0E takes into account the stages 1 and 2 are by-passed. See Figure 4-16 for "dual-channel Input" for DDC.
7: This decimation value is from the decimation filter. When DDC is used, the actual total decimation is 2x larger since 2x is included from the DDC Half-Band Filter. Example: "Dual-Ch., Decimation = 8x, DDC-f_S/8" option actually has 16x decimation with 8x provided by the decimation filter and 2x by the DDC Half-Band Filter.

TABLE 4-18: OUTPUT TYPE VS. CONTROL PARAMETERS FOR DUAL-CHANNEL DDC – EXAMPLE

Output Type	Control Parameter	Register	Descriptions
Complex: I and Q	EN_DSPPDUAL = 1	0x79	Enable all digital post-processing functions for dual-channel operations
	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	HBFILTER_B = 1	0x80	Enable Half-Band Filter B, includes 2x decimation
	EN_DDC_FS/8 = 0	0x81	NCO (f_S/8/DER) is disabled
	EN_DDC2 = 0	0x80	DDC2 is disabled
	FIR_A<8:1> = 0x00	0x7B	FIR A decimation filter is disabled
	FIR_B<7:0> = 0x00	0x7C	FIR B decimation filter is disabled
	OUT_CLKRATE<3:0>	0x02	Output clock rate is not affected (no need to change)
Real: $Real_A$ for Channel A and $Real_B$ for Channel B after NCO (f_S/8/DER) without using Decimation Filter	EN_DSPPDUAL = 1	0x79	Enable all digital post-processing functions for dual-channel operations
	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	HBFILTER_B = 1	0x80	Enable Half-Band Filter B, includes 2x decimation
	EN_DDC_FS/8 = 1	0x81	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8 (**Note 1**).
	EN_DDC2 = 1	0x80	DDC2 is enabled
	FIR_A<8:1> = 0x00	0x7B	Decimation filter FIR A is disabled
	FIR_B<7:0> = 0x00	0x7C	Decimation filter FIR B is disabled
	OUT_CLKRATE<3:0> = 0001	0x02	Adjust the output clock rate to divided by 2 (**Note 2**)
Decimated Real: $Real_{A\_DEC}$ for Channel A and $Real_{B\_DEC}$ for Channel B after NCO (f_S/8/DER) and Decimation Filter	EN_DSPPDUAL = 1	0x79	Enable all digital post-processing functions for dual-channel operation
	EN_DDC1 = 1	0x80	Enable DDC1 block
	EN_NCO = 1	0x80	Enable 32-bit NCO
	HBFILTER_A = 1	0x80	Enable Half-Band Filter A, includes 2x decimation
	HBFILTER_B = 1	0x80	Enable Half-Band Filter B, includes 2x decimation
	EN_DDC_FS/8 = 1	0x81	NCO (f_S/8/DER) is enabled. This translates the input signal from DC to f_S/8/DER (**Note 1**).
	EN_DDC2 = 1	0x80	DDC2 is enabled
	FIR_A<8:1>	0x7B	Program FIR A filter for extra decimation (**Note 3**)
	FIR_B<7:0>	0x7C	Program FIR B filter for extra decimation (**Note 3**)
	OUT_CLKRATE<3:0>	0x02	Adjust the output clock rate to the total decimation rate including the 2x decimation by the Half-Band Filter A

Note 1: DER is the decimation rate setting of FIR A and FIR B filters.

2: Divided by 2 is due to the 2x decimation included in the Half-Band Filter A.

3: When this filter is used, the up-conversion frequency is reduced by the extra decimation rates (DER).

4.9 Digital Offset and Digital Gain Settings

Offset and gain can be individually adjusted for each input channel. Figure 4-22 shows a simplified block diagram of the digital offset and gain settings. Offset is applied prior to the gain.

Offset and gain adjustments occur prior to DDC, Decimation or FDR when these features are used.

4.9.1 DIGITAL OFFSET SETTINGS

The offset of an individual channel can be controlled using CH(N)_DIG_OFFSET<7:0> in Addresses 0x9E – 0xA7 (Registers 5-71 – 5-79) together with the offset weight control register, DIG_OFFSET_WEIGHT<1:0> in 0xA7 (Register 5-79).

Note that, except for the octal-channel mode, the offset setting registers, 0x9E – 0xA7 (Registers 5-71 – 5-79), do not sequentially correspond to the channel order defined by CH_ORDER<23:0>. Table 4-19 shows the details of the offset registers that correspond to the actual channels, depending on the number of channels used.

4.9.2 DIGITAL GAIN SETTINGS

CH(N)_DIG_GAIN<7:0> in Addresses 0x96 – 0x9D (Registers 5-63 – 5-70) is used to adjust the digital gain per channel.

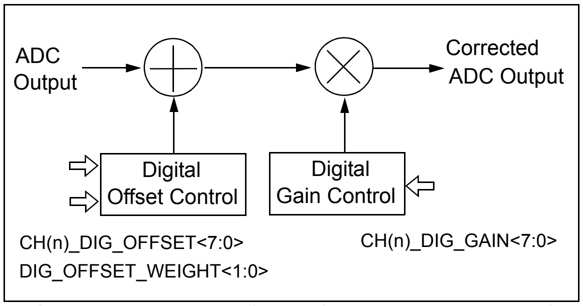


FIGURE 4-22: *Simplified Block Diagram for Digital Offset and Gain Settings.*

Note 1: Digital Offset Setting: register mapping (0x9E – 0xA7) to the corresponding channel is not sequential to the channel order defined by CH_ORDER<23:0>, except for the octal-channel mode. See Table 4-19 for details.

2: Gain and NCO Phase Offset: register mapping to the corresponding channel is sequential to the channel order defined by CH_ORDER<23:0>.

TABLE 4-19: REGISTER ASSIGNMENT FOR OFFSET SETTING

Number of Channel Used	Register Address for Offset Setting							
	1st Channel	2nd Channel	3rd Channel	4th Channel	5th Channel	6th Channel	7th Channel	8th Channel
1	0x9F	—	—	—	—	—	—	—
2	0xA0	0x9F	—	—	—	—	—	—
3	0xA1	0x9F	0xA0	—	—	—	—	—
4	0xA2	0x9F	0xA0	0xA1	—	—	—	—
5	0xA3	0x9F	0xA0	0xA1	0xA2	—	—	—
6	0xA4	0x9F	0xA0	0xA1	0xA2	0xA3	—	—
7	0xA5	0x9F	0xA0	0xA1	0xA2	0xA3	0xA4	—
8	0x9E	0x9F	0xA0	0xA1	0xA2	0xA3	0xA4	0xA5

4.10 Continuous Wave (CW) Beamforming and Ultrasound Doppler-Signal Processing Using CW Octal-Channel Mode (MCP37D11-200 Only)

In modern ultrasound medical applications, large numbers of transducers are often used. The signals from these sensors are then coherently combined for higher transducer gain and directivity. The signals from each sensor arrive at the detection device with a different time delay. Also, in multi-channel scanning operations using the MUX, there is a time delay between acquiring input signals (see **Section 4.8.1 "Fractional Delay Recovery for Dual and Octal-Channel Modes"**). These time delays may need to be corrected before all input signals are combined for the signal processing.

Digital beamforming is a digital signal-processing technique that requires summing all input signals from different channels after correcting for time delay. The time delay correction involves the phase alignment of the detected signals with respect to a reference.

Along with the beamforming, many modern medical ultrasound devices support Doppler imaging which processes phase information in addition to the classical magnitude detection (for brightness imaging). The ultrasound Doppler signal processing is used to determine movement in the body as represented by blood flow, which can help to diagnose the functioning of a heart valve or blood vessel, etc. In a traditional ultrasound system, all of these functions are typically accomplished with discrete components. Figure 4-24 shows an example of an ultrasound system implementation using various specialized components.

The MCP37D11-200 device has a built-in feature that can perform some of the functions that are done traditionally using extra components. The continuous wave (CW) digital beamforming and Doppler signal processing features are available, but these are offered in the octal-channel operation only.

Figure 4-23 shows a simplified block diagram for the ultrasound CW beamingforming with DDC I/Q decimation. Note that the sub-blocks shown after the MUX are commonly used for all input channels.

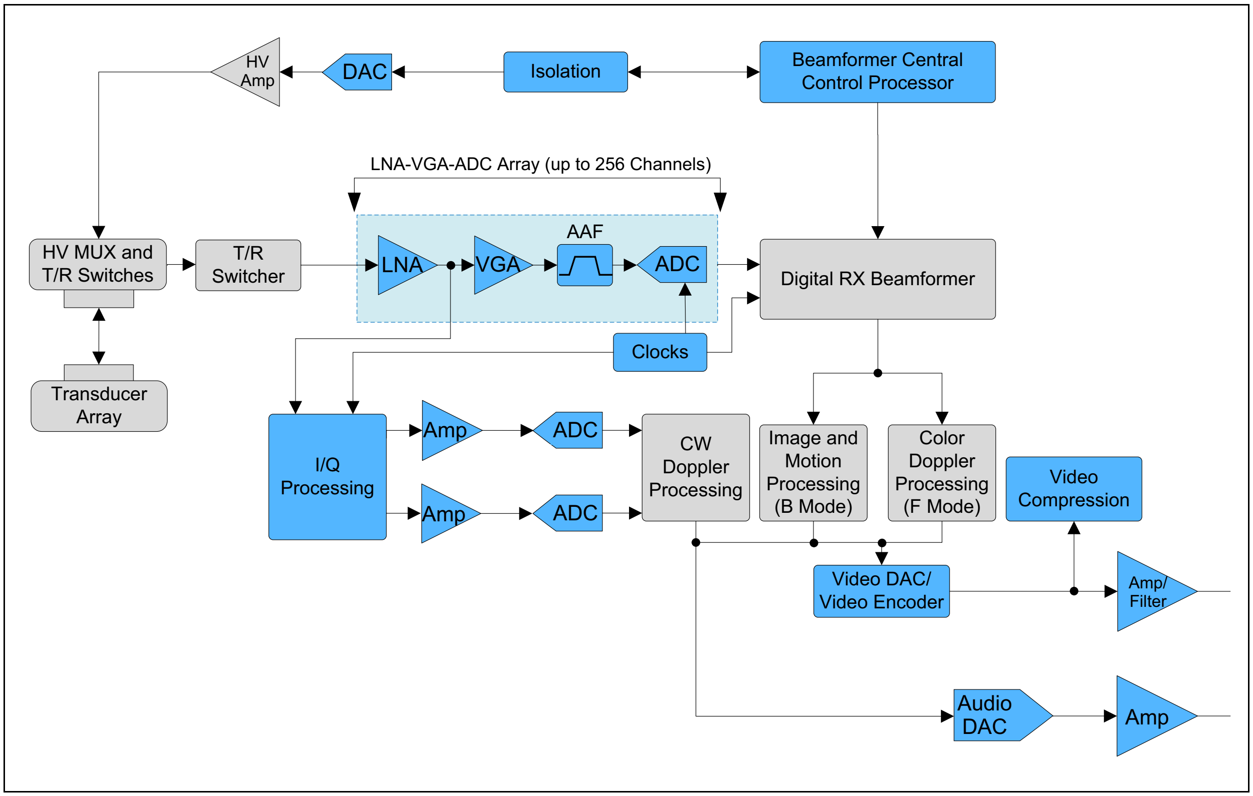


FIGURE 4-23: *Example of Ultrasound System Building Block.*

4.10.1 BEAMFORMING

Beamforming is achieved by scanning all inputs while correcting the phase of each channel with respect to a reference. This can be done using:

- Fractional Delay Recovery (FDR)
- Phase offset settings of each individual channel
- Gain setting per channel

While the CW input channel is multiplexed sequentially, the phase offset can be added to the NCO output (each channel individually). CH(n)_NCO_PHASE<15:0>, in Addresses 0x86 to 0x95 (Registers 5-47 – 5-62), corrects the time delay of the incoming signals with respect to the reference.

The phase-compensated input signal is then down-converted by a wide dynamic range I/Q demodulator. The digital beamforming of the inputs is then obtained by summing I and Q data from individual channels. This summed I and Q data are fed to the half-band filter. Equation 4-10 shows the I and Q data of an individual channel with phase correction (phase offset) and the resulting digital beamforming signal.

The processing blocks after the digital beamforming are the same as for the DDC single-channel operation described in **Section 4.8.4.1 "Single-Channel DDC"**, except only limited decimation rates of the FIR A and FIR B filters are used due to the processing time requirement for summing of the input signals from all channels.

EQUATION 4-10: BEAMFORMING SIGNALS

$$I_{CH(n)} = ADC \times COS(2\pi f_{NCO}t + \phi(n))$$

$$Q_{CH(n)} = ADC \times SIN(2\pi f_{NCO}t + \phi(n))$$

$$I = \sum_{n=0}^{N} I_{CH(n)}$$

$$Q = \sum_{n=0}^{N} Q_{CH(n)}$$

$$\phi(n) = 360^{\circ} \times \frac{CH(n)\_NCO\_PHASE<15:0>}{2^{16}}$$

$$= 0.005493164^{\circ} \times CH(n)\_NCO\_PHASE<15:0>$$

Where:

ϕ(n) = NCO phase offset of channel *n*
ADC = the output of the ADC block

The NCO phase offset can be controlled by 0.005493164° per step. See **Section 4.8.4.7 "NCO Phase Offset Control"** for details.

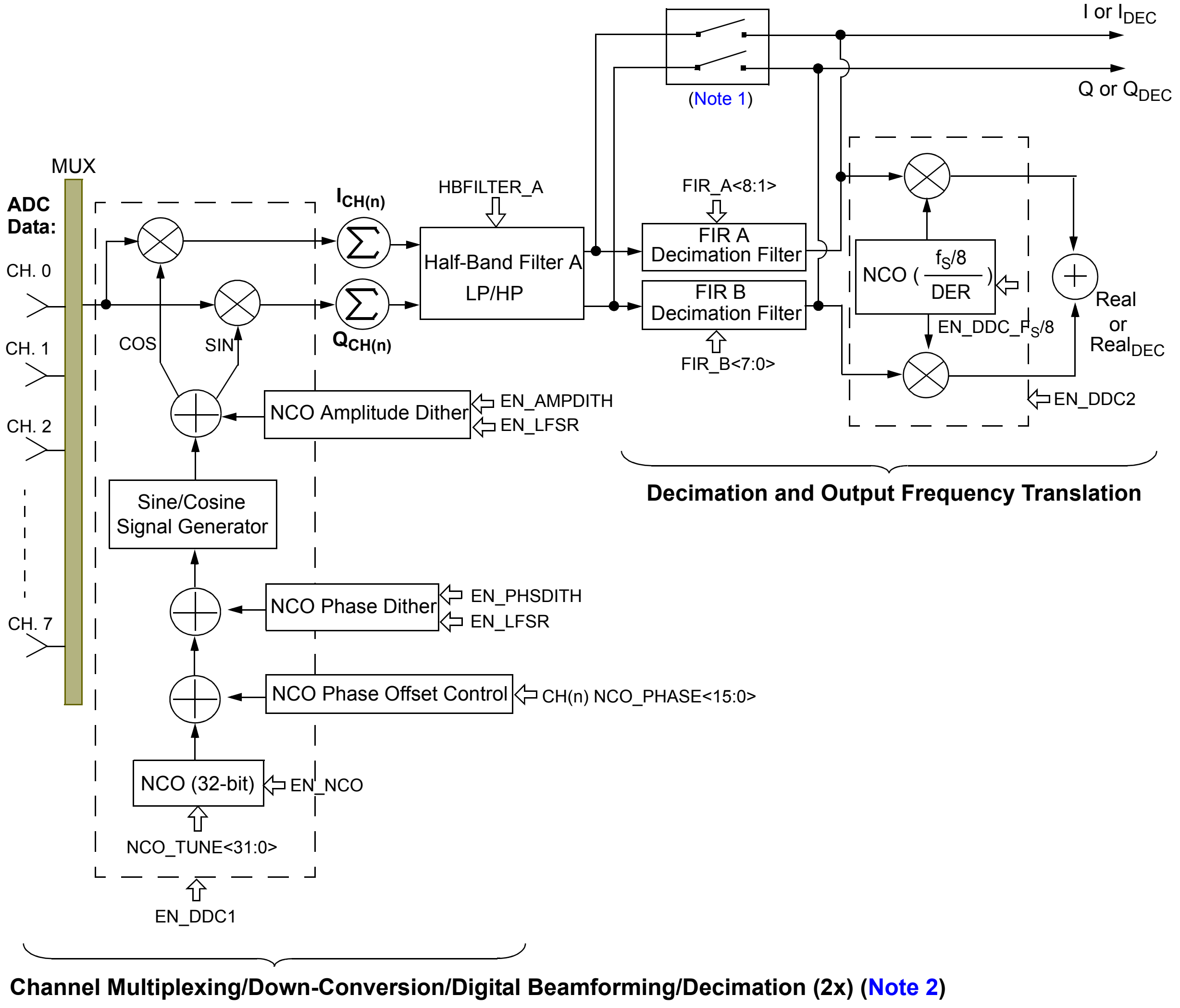
4.10.2 ULTRASOUND DOPPLER SIGNAL PROCESSING

Doppler shift measurement requires summing the input signals from multiple transducer channels and mixing them with a phase-controlled local oscillator frequency. The resulting low-frequency output is then centered near DC and can measure a Doppler shift produced by moving objects, such as blood flow and changes in blood pressure in arteries, etc. In traditional Doppler measurements, many discrete analog components are used along with, typically, a high-resolution ADC (~18-bit range).

This device has unique built-in features that are suitable for ultrasound Doppler shift measurements. By utilizing these features, system engineers can reduce many discrete components which are otherwise necessary for an ultrasound Doppler measurement system.

The following built-in digital signal post-processing (DSPP) features in the MCP37D11-200 can be effectively used for the ultrasound Doppler signal processing applications:

- **Fractional Delay Recovery (FDR):** correct the time delay of signal sampling between channels. See **Section 4.8.1 "Fractional Delay Recovery for Dual and Octal-Channel Modes"** for details,
- **Digital Gain and Offset adjustment for each channel:** see **Section 4.9 "Digital Offset and Digital Gain Settings"** for details.
- **Down-conversion for each channel** with a unique phase of the same NCO frequency prior to summing the eight channels as shown in Figure 4-24.
- After down-conversion by the DDC, the resulting signal can then be decimated to achieve very high SNR in a narrow bandwidth.



Channel Multiplexing/Down-Conversion/Digital Beamforming/Decimation (2x) (Note 2)

Note 1: Switches are closed if decimation filter is not used and open if decimation filter is used.

2: Digital Gain and Offset adjustment are applied prior to digital down-conversion and are not shown here.

FIGURE 4-24: *Simplified Block Diagram of CW Beamforming and I/Q Signal Processing – Available in MCP37D11-200 Only.*

4.11 Digital Output

The MCP37211-200 and MCP37D11-200 can operate in one of two digital output modes:

- Full Rate CMOS
- Double Data Rate (DDR) LVDS

The outputs are powered by DV_{DD18} and GND. LVDS mode is recommended for data rates above 80 Msps. The digital output mode is selected by the OUTPUT_MODE<1:0> bits in Address 0x62 (Register 5-20). Figures 2-1 – 2-2 show the timing diagrams of the digital output.

4.11.1 FULL RATE CMOS MODE

In full-rate CMOS mode, the data outputs (Q11 to Q0), over-range indicator (OVR), word clock (WCK) and the data output clock (DCLK+, DCLK–) have CMOS output levels. The digital output should drive minimal capacitive loads. If the load capacitance is larger than 10 pF, a digital buffer should be used.

4.11.2 DOUBLE DATA RATE LVDS MODE

The double data rate (DDR) LVDS output is a parallel data stream which changes on each edge of the output clock. See Figure 2-2 for details.

The digital output data is clocked out through six LVDS output pairs (Q5+/Q5- through Q0+/Q0-). Word clock and over-range (WCK/OVR) and digital output clock (DCLK+/DCLK–) are also LVDS output pairs.

In multi-channel configuration, the data is output sequentially with the WCK that is synchronized to the first sampled channel.

A 100Ω differential termination resistor is required for each LVDS output pin pair. The termination resistor should be located as close as possible to the LVDS receiver. By default, the outputs are standard LVDS levels: 3.5 mA output current with a 1.15V output common-mode voltage on 100Ω differential load. See Address 0x63 (Register 5-21) for more details on the LVDS mode control.

Note: LVDS output polarity can be controlled independently for each LVDS pair. See POL_LVDS<7:0> setting in Address 0x65 (Register 5-23).

Note: **Output Data Rate in LVDS Mode:** In octal-channel mode, the input sample rate per channel is $f_S/8$. The output data rate to shift out the 12-bit data of all the eight channels in DDR is still equivalent to f_S. For example, if $f_S = 200$ Msps, each channel's sample rate is $f_S/8 = 25$ Msps and the output clock rate (DCLK) for 12-bit DDR output is 200 MHz.

4.11.3 PROGRAMMABLE LVDS OUTPUT CURRENT

In LVDS mode, the default output driver current is 3.5 mA. This current can be adjusted by using LVDS_IMODE<2:0> bit setting in Address 0x63 (Register 5-21). Available output drive currents are 1.8 mA, 3.5 mA, 5.4 mA and 7.2 mA.

4.11.4 OPTIONAL LVDS DRIVER INTERNAL TERMINATION

In most cases, using an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by setting the LVDS_LOAD bit in Address 0x63 (Register 5-21). The internal termination helps absorb any reflections caused by imperfect impedance termination at the receiver.

4.11.5 OVER-RANGE BIT (OVR)

The input over-range status bit is asserted (logic high) when the analog input has exceeded the full-scale range of the ADC in either the positive or negative direction. In LVDS DDR output mode, the OVR bit is multiplexed with the word clock (WCK) output bit, such that OVR is output on the falling edge of the data output clock and WCK on the rising edge.

The OVR bit has the same pipeline latency as the ADC data bits. In multi-channel mode, the OVR is output independently for each input channel and is synchronized to the data. See Address 0x68 (Register 5-26) for OVR and WCK control options.

If DSPP options are enabled, OVR pipeline latency will be unaffected, however the data will incur additional delay. This has the effect of allowing the OVR indicator to precede the affected data.

4.11.6 WORD CLOCK (WCK)

The word clock output bit indicates the start of a new data set. In single-channel mode, this bit is disabled. In DDR output with multi-channel mode, it is always asserted coincidentally with the data from the first sampled channel and multiplexed with the OVR bit. See Address 0x68 (Register 5-26) for OVR and WCK control options.

4.12 Output Data format

The device can output the ADC data in offset binary or two's complement. The data format is selected by the DATA_FORMAT bit in Address 0x62 (Register 5-20). Table 4-20 shows the relationship between the analog input voltage, the digital data output bits and the over-range bit. By default, the output data format is two's complement.

TABLE 4-20: ADC OUTPUT CODE VS. INPUT VOLTAGE

Input Range	Offset Binary (1)	Two's Complement (1)	Over-Range (OVR)
$A_{IN} > A_{FS}$	1111-1111-1111	0111-1111-1111	1
$A_{IN} = A_{FS}$	1111-1111-1111	0111-1111-1111	0
$A_{IN} = A_{FS} – 1$ LSB	1111-1111-1110	0111-1111-1110	0
$A_{IN} = A_{FS} – 2$ LSB	1111-1111-1100	0111-1111-1100	0
• • •			
$A_{IN} = A_{FS}/2$	1100-0000-0000	0100-0000-0000	0
$A_{IN} = 0$	1000-0000-0000	0000-0000-0000	0
$A_{IN} = -A_{FS}/2$	0011-1111-1111	1011-1111-1111	0
• • •			
$A_{IN} = -A_{FS} + 2$ LSB	0000-0000-0010	1000-0000-0010	0
$A_{IN} = -A_{FS} + 1$ LSB	0000-0000-0001	1000-0000-0001	0
$A_{IN} = -A_{FS}$	0000-0000-0000	1000-0000-0000	0
$A_{IN} < - A_{FS}$	0000-0000-0000	1000-0000-0000	1

Note 1: MSB is sign bit.

4.12.1 PHASE SHIFTING OF OUTPUT CLOCK (DCLK)

In full rate CMOS mode, the data output bit transition occurs at the rising edge of DCLK+. In double data rate LVDS mode, the data transition occurs at both the rising and falling edges of DCLK+. For adequate setup and hold time when latching the data into the external host device, the user can adjust the phase of the digital clock output (DCLK+, DCLK-), relative to the data output bits.

This digital output clock (DCLK+, DCLK-) phase delay can be achieved by using the phase delay control registers. Table 4-21 shows the output clock phase control registers. Figure 4-25 shows an example of the output clock phase delay control using the DLL_PHDLY<2:0> in DLL block (PLL and decimation are not used).

TABLE 4-21: OUTPUT CLOCK (DCLK) PHASE CONTROL PARAMETERS

Control Parameter	Register	Operating Condition
DLL_PHDLY<2:0>	0x52	External clock is used as timing source without using PLL or decimation.The phase delay is controlled in DLL Block. See Figure 4-11 for details.
PLL_PHDLY<3:0>	0x6D	PLL is used without using decimation. The phase delay is controlled in PLL Block. Figure 4-11 for details.
DCLK_PHDLY_DEC<2:0>	0x64	The decimation filter is used. See **Section 4.8.3 "Decimation Filters"** for details.

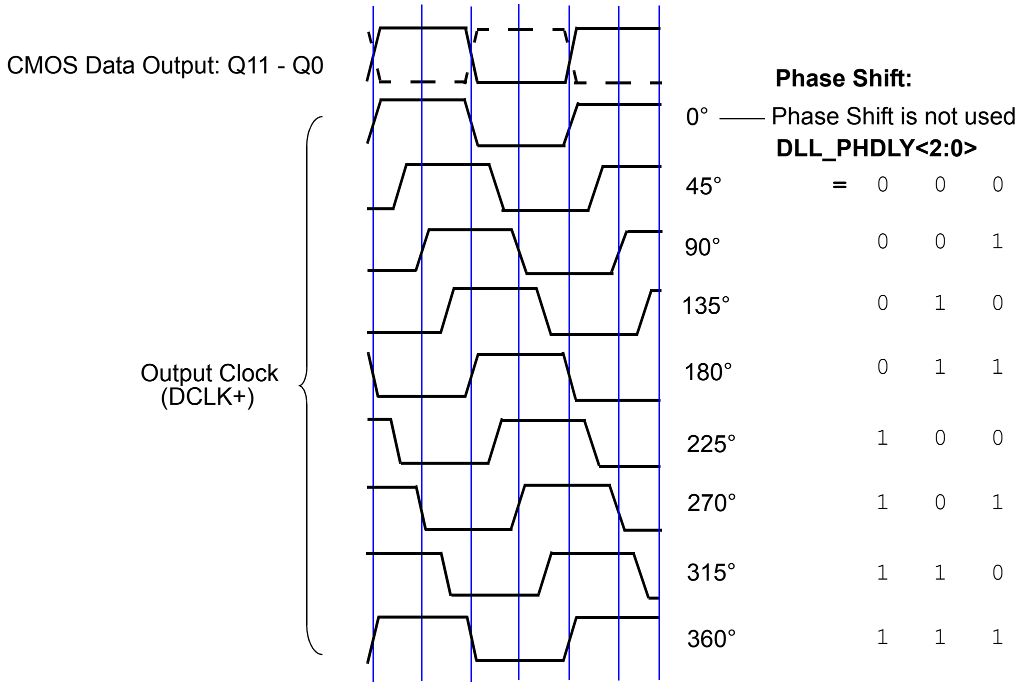


FIGURE 4-25: Phase Shifting of Digital Output Clock (DCLK).

4.13 Digital Output Randomizer

Depending on PCB considerations and power supply coupling, SFDR may be improved by decorrelating the ADC input from the ADC digital output data. The device includes an output data randomizer option. When this option is enabled, the digital output is randomized by applying an exclusive-OR logic operation between the LSB(Q0) and all other data output bits.

To decode the randomized data, the reverse operation is applied: an exclusive-OR operation is applied between the LSB(Q0) and all other bits. The DCLK, OVR, WCK and LSB(Q0) outputs are not affected. Figure 4-26 shows the block diagram of the data randomizer and decoder logic. The output randomizer is enabled by setting the EN_OUT_RANDOM bit in Address 0x07 (Register 5-5).

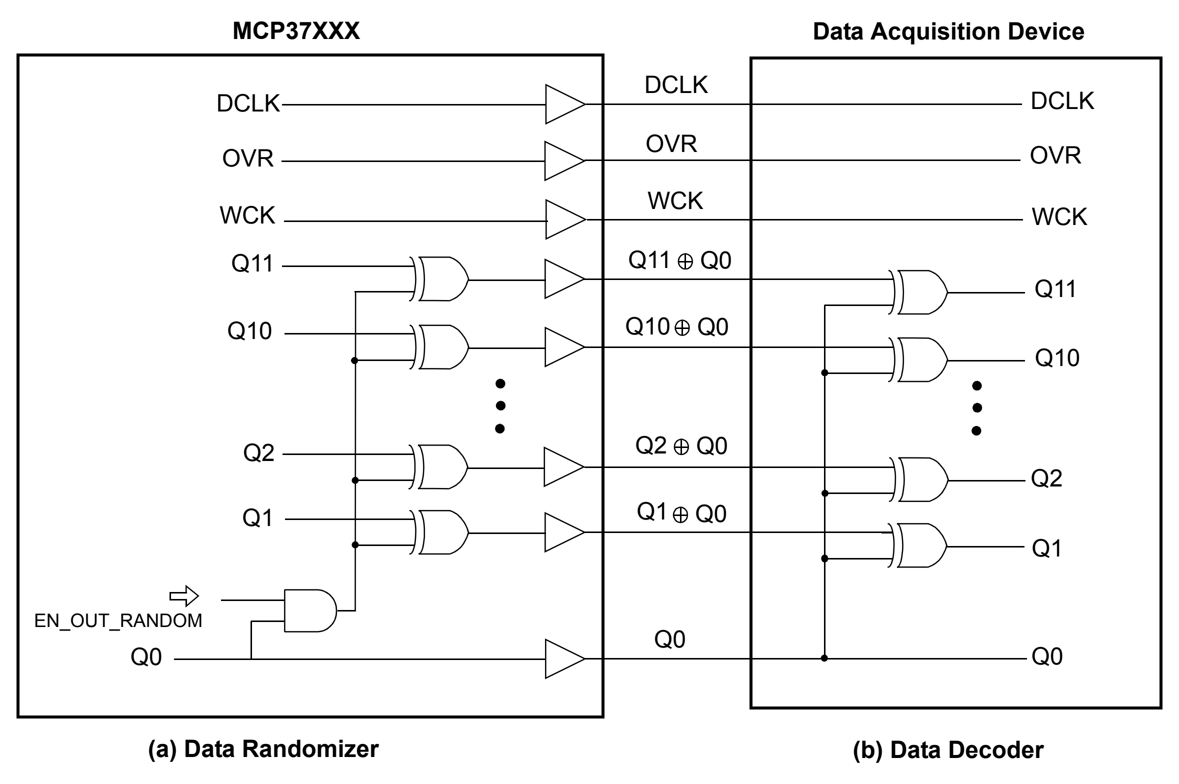


FIGURE 4-26: *Logic Diagram for Digital Output Randomizer and Decoder.*

4.14 Output Disable

The digital output can be disabled by setting OUTPUT_MODE<1:0> = `00` in Address 0x62 (Register 5-20). All digital outputs are disabled, including OVR, WCK, DCLK, etc.

4.15 Output Test Patterns

To facilitate testing of the I/O interface, the device can produce various predefined or user-defined patterns on the digital outputs. See TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20) for various output test pattern selection. For the user-defined patterns, the Addresses 0x74 – 0x77 (Registers 5-29 – 5-32) can be programmed using the SPI interface. When an output test mode is enabled, the ADC analog section can still be operational, but does not drive the digital outputs. The outputs are driven only with the selected test pattern.

Since the output test pins (TP) can toggle during this test, always leave the TP pins floating (not connected) to avoid contention and excess current draw.

4.15.1 PSEUDO-RANDOM NUMBER (PN) SEQUENCE OUTPUT

When TEST_PATTERNS<2:0> = `111`, the device outputs a pseudo-random number (PN) sequence which is defined by the polynomial of degree 16, as shown in Equation 4-11. Figure 4-27 shows the block diagram of a 16-bit Linear Feedback Shift Register (LFSR) for the PN sequence.

EQUATION 4-11: POLYNOMIAL FOR PN

$$P(x) = 1 + x^4 + x^{13} + x^{15} + x^{16}$$

The output PN[15:4] is directly applied to the output pins Qn[11:0]. In addition to the output at the Qn[11:0] pins, the two MSBs, PN[15] and PN[14] are copied to OVR and WCK pins, respectively.

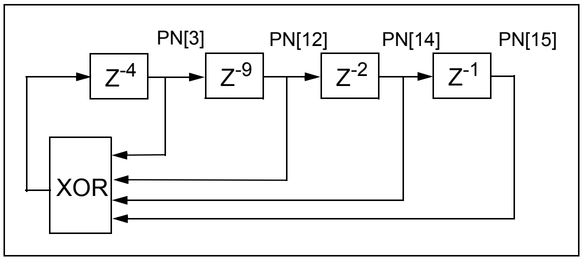


FIGURE 4-27: *Block Diagram of 16-Bit LFSR for Pseudo-Random Number (PN) Sequence for Output Test Pattern.*

4.16 System Calibration

The built-in system calibration algorithm includes:

- Harmonic Distortion Correction (HDC)
- DAC Noise Cancellation (DNC)
- Dynamic Element Matching (DEM)

HDC and DNC correct the nonlinearity in the residue amplifier and DAC, respectively. The system calibration is performed by:

- Power-up calibration, which takes place during the power-on reset sequence (requires 2^{27} clock cycles)
- Background calibration, which takes place during normal operation (per 2^{30} clock cycles)

Background calibration time is invisible to the user and primarily affects the ADC's ability to track variations in ambient temperature.

The calibration status is monitored by CAL pin or the CAL_STAT bit in Address 0xC0 (Register 5-80). See also Address 0x07 (Register 5-5) and 0x1E (Register 5-6) for time delay control of the auto-calibration. Table 4-22 shows the calibration time for various ADC core sample rates.

TABLE 4-22: CALIBRATION TIME VS. ADC CORE SAMPLE RATE

f_S (Msps)	200	150	100	70	50
Power-Up Calibration Time (s)	0.67	0.9	1.34	1.92	2.68
Background Calibration Time (s)	5.37	7.16	10.73	15.34	21.48

4.16.1 RESET COMMAND

Although the background calibration will track changes in temperature or supply voltage, changes in clock frequency or register configuration should be followed by a recalibration of the ADC. This can be accomplished either via the Hard or Soft Reset commands. The recalibration time is the same as the power-up calibration time (2^{27} clock cycles). During the reset, the device has the following state:

- No ADC output
- No change in power-on condition of internal reference
- Most of the internal clocks are not distributed
- Contents of internal user registers:
  - Not affected by Soft Reset
  - Reset to default values by Hardware Reset
- Current consumption of the digital section is negligible, but no change in the analog section

4.16.1.1 Hardware Reset

A hard reset is triggered by toggling the $\overline{\text{RESET}}$ pin. On the rising edge, the internal user registers are initialized to their default states and recalibration of the ADC commences. The recalibration time is the same as the power-up calibration time. See Figure 2-6 for the timing details of the hardware $\overline{\text{RESET}}$ pin.

4.16.1.2 Soft Reset

The user can issue a Soft Reset command for a fast recalibration of the ADC, by setting the $\overline{\text{SOFT\_RESET}}$ bit to ‘`0`’ in Address 0x00 (Register 5-1). During Soft Reset, all internal calibration registers are initialized to their initial default states. User registers are unaffected. When exiting the Soft Reset (changing from ‘`0`’ to ‘`1`’), an automatic device calibration takes place.

4.17 Power Dissipation and Power Savings

The power dissipation of the ADC core is proportional to the sample rate (f_S). The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load condition on each output pin. The maximum digital load current (I_{LOAD}) can be calculated as:

EQUATION 4-12: CMOS OUTPUT LOAD CURRENT

$$I_{LOAD} = DV_{DD1.8} \times f_{DCLK} \times N \times C_{LOAD}$$

Where:

N = Number of bits
C_{LOAD} = Capacitive load of output pin

The capacitive load presented at the output pins needs to be minimized to minimize digital power consumption. The output load current of the LVDS output is constant, since it is set by LVDS_IMODE<2:0> in Address 0x63 (Register 5-21).

4.17.1 POWER SAVING MODES

This device has two power-saving modes:

- Shutdown
- Standby

They are set by the SHUTDOWN and STANDBY bits in Address 0x00 (Register 5-1).

In Shutdown mode, most of the internal circuitry, including the reference and clock, are turned off with the exception of the SPI interface. During Shutdown, the device consumes 25 mA (typical), primarily due to digital leakage. When exiting Shutdown, issuing a Soft Reset at the same time is highly recommended. This will perform a fast recalibration of the ADC. The contents of the internal registers are not affected by the Soft Reset.

In Standby mode, most of the internal circuitry is disabled except for the reference, clock and SPI interface. If the device has been in standby for an extended period of time, the existing calibration may not be accurate. Therefore, when exiting from Standby mode, executing the device Soft Reset at the same time is highly recommended.

5.0 SERIAL PERIPHERAL INTERFACE (SPI)

The user can configure the ADC for specific functions or optimized performance by setting the device's internal registers through the serial peripheral interface (SPI). The SPI communication uses three pins: $\overline{\text{CS}}$, SCLK and SDIO. Table 5-1 summarizes the SPI pin functions. The SCLK is used as serial timing clock and can be used up to 50 MHz. SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent or read from the internal registers. The Chip Select ($\overline{\text{CS}}$) pin enables the SPI communication when active-low. The falling edge of $\overline{\text{CS}}$ followed by a rising edge of SCLK determines the start of the SPI communication. When $\overline{\text{CS}}$ is tied to high, the SPI communication is disabled and SPI pins are placed in high-impedance mode. The internal registers are accessible by their address.

Figures 5-1 and 5-2 show the SPI data communication protocols for this device with MSB-first and LSB-first option, respectively. It consists of:

- 16-bit wide instruction header + Data byte 1 + Data byte 2 + . . . + Data Byte N

Table 5-2 summarizes the bit functions. The R/$\overline{\text{W}}$ bit of the instruction header indicates whether the command is a read (‘`1`’) or a write (‘`0`’):

- If the R/$\overline{\text{W}}$ bit is ‘`1`’, the SDIO pin changes direction from an input (SDI) to an output (SDO) after the 16-bit wide instruction header.

By selecting the R/$\overline{\text{W}}$ bit, the user can write the register or read back the register contents. The W1 and W2 bits in the instruction header indicate the number of data bytes to transmit or receive in the following data frame.

A2 – A0 bits are the SPI device address bits. These bits are used when multiple devices are used in the same SPI bus. A2 is internally hardcoded to ‘`0`’. A1 and A0 bits correspond to the logic level of ADR1 and ADR0 pins, respectively.

Note: In VTLA-124 package, ADR1 is internally bonded to ground (logic ‘`0`’).

The R9 – R0 bits represent the starting address of the configuration register to write or read. The data bytes following the instruction header are the register data. All register data is 8-bit wide. Data can be sent in MSB-first mode (default) or in LSB-first mode, which is determined by <LSB_ FIRST> bit setting in Address 0x00 (Register 5-1). In the Write mode, the data is clocked in at the rising edge of the SCLK. In the Read mode, the data is clocked out at the falling edge of the SCLK.

TABLE 5-1: SPI PIN FUNCTIONS

Pin Name	Descriptions
$\overline{\text{CS}}$	Chip Select pin. SPI mode is initiated at the falling edge. It needs to maintain active-low for the entire period of the SPI communication. The device exits the SPI communication at the rising edge.
SCLK	Serial clock input pin. • Writing to the device: data is latched at the rising edge of SCLK • Reading from the device: data is latched at the falling edge of SCLK
SDIO	Serial data input/output pin. This pin is initially input pin (SDI) during the first 16-bit instruction header. After the instruction header, its I/O status can be changed depending on the R/$\overline{\text{W}}$ bit: • if R/$\overline{\text{W}}$ = `0`: data input pin (SDI) for writing • if R/$\overline{\text{W}}$ = `1`: data output pin (SDO) for reading

TABLE 5-2: SPI DATA PROTOCOL BIT FUNCTIONS

Bit Name	Descriptions
R/$\overline{\text{W}}$	`1` = Read Mode `0` = Write Mode
W1, W0 (Data Length)	`00` = Data for one register (1 byte) `01` = Data for two registers (2 bytes) `10` = Data for three registers (3 bytes) `11` = Continuous reading or writing by clocking SCLK (**Note 1**).
A2 – A0	Device SPI Address for multiple devices in SPI bus. A2: Internally hardcoded to ‘`0`’ A1: Logic level of ADR1 pin A0: Logic level of ADR0 pin
R9 – R0	Address of starting register
D7 – D0	Register data. MSB or LSB first, depending on LSB_FIRST bit setting in 0x00.

Note 1: The register address counter is incremented by one per step. The counter does not automatically reset to 0x00 after reaching the last address (0x15F). The user also needs to be aware the user registers are not sequentially allocated.

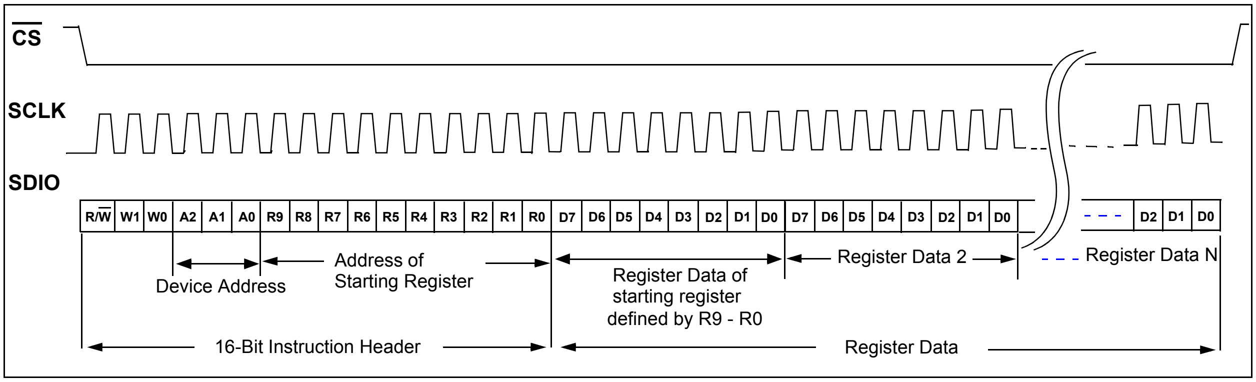


FIGURE 5-1: *SPI Serial Data Communication Protocol with MSB-First. See Figures 2-5 and 2-6 for Timing Specifications.*

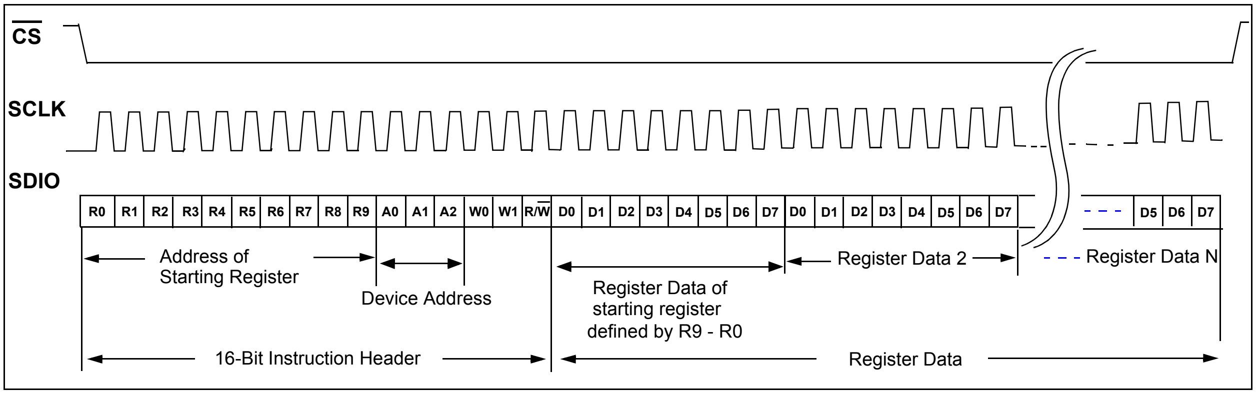


FIGURE 5-2: *SPI Serial Data Communication Protocol with LSB-First. See Figures 2-5 and 2-6 for Timing Specifications.*

5.1 Register Initialization

The internal configuration registers are initialized to their default values under two different conditions:

- After 2^{20} clock cycles of delay from the power-on reset (POR).
- By the hardware reset pin ($\overline{\text{RESET}}$).

Figures 2-5 and 2-6 show the timing details.

5.2 Configuration Registers

The internal registers are mapped from address 0x00 to 0x15F. Among them, 83 registers are user configuration registers. These user registers are not sequentially located, but mixed with factory-controlled registers. Some user configuration registers also have factory-controlled bits. The factory-controlled registers and bits cannot be overwritten by the user. All user configuration registers are read/write, except for the last four registers, which are read-only. Each register is made of an 8-bit wide volatile memory and their default values are loaded during the power-up sequence or by using the hardware $\overline{\text{RESET}}$ pin. All registers are accessible by the SPI command using the register address. Table 5-3 shows the user configuration memory map and Registers 5-1 – 5-83 show the details of the register bit functions.

Note 1: All address and bit locations that are not included in the following table should not be written or modified by the user. Contact Microchip Technology Inc. for more information on the factory programming bit settings.

2: Some registers include factory-controlled bits (FCB). Do not overwrite these bits.

TABLE 5-3: REGISTER MAP TABLE

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x00	SPI Bit Ordering and ADC Mode Selection	SHUTDOWN 1 = Shutdown	LSB-First 1 = LSB first 0 = MSB first	$\overline{\text{SOFT\_RESET}}$ 0 = Soft Reset	STANDBY 1 = Standby	STANDBY 1 = Standby	$\overline{\text{SOFT\_RESET}}$ 0=Soft Reset	LSB-First 1 = LSB first 0 = MSB first	SHUTDOWN 1 = Shutdown	0x24
0x01	No. of Channel Selection and Independence Control of Output Data and Clock Divider	EN_DATCLK_IND	FCB<3> = 0	SEL_NCH<2:0>			FCB<2:0> = 111			0x0F
0x02	Output Data and Clock Rate	OUT_DATARATE<3:0>				OUT_CLKRATE<3:0>				0x00
0x04	SPI SDO Timing Control	SDO_TIME	FCB<6:0> = 001111							0x9F
0x07	Output Randomizer and WCK Polarity	POL_WCK	EN_AUTOCAL_ TIMEDLY	FCB<4:0> = 100001					EN_OUT_ RANDOM	0x62
0x1E	Auto-Calibration Time Delay	AUTOCAL_TIMEDLY<7:0>								0x80
0x52	DLL Control	EN_DUTY	DLL_PHDLY<2:0>			EN_DCLK	EN_DLL	EN_CLK	$\overline{\text{RESET\_DLL}}$	0x0A
0x53	Clock Source Selection	FCB<6:4>= 001			CLK_SOURCE	FCB<3:0>= 0101				0x45
0x54	PLL Reference Divisor	PLL_REFDIV<7:0>								0x00
0x55	PLL Output and Reference Divisor	PLL_OUTDIV<3:0>				U<1:0>		PLL_REFDIV<9:8>		0x40
0x56	PLL Prescaler (LSB)	PLL_PRESCALER (LSB)<7:0>								0x78
0x57	PLL Prescaler (MSB)	FCB<3:0> = 0100				PLL_PRESCALER (MSB)<11:8>				0x40
0x58	PLL Charge Pump	FCB<2:0> = 001			PLL_BIAS	PLL_CHAGPUMP<3:0>				0x22
0x59	PLL Enable Control 1	U	FCB<4:3> = 1000		EN_PLL_REVDIV	FCB<2:1>		EN_PLL	FCB<0> = 1	0x41
0x5A	PLL Loop Filter Resistor	U	FCB<1:0> = 01		PLL_RES<4:0>					0x2F
0x5B	PLL Loop Filter Cap3	U	FCB<1:0> = 01		PLL_CAP3<4:0>					0x27
0x5C	PLL Loop Filter Cap1	U	FCB<1:0> = 01		PLL_CAP1<4:0>					0x27
0x5D	PLL Loop Filter Cap2	U	FCB<1:0> = 01		PLL_CAP2<4:0>					0x27
0x5F	PLL Enable Control 2	FCB<7:4>				EN_PLL_OUT	EN_PLL_BIAS	FCB<1:0>		0xF1
0x62	Output Data Format and Output Test Patterns	U	FCB<0>	DATA_FORMAT 1 = Offset binary 0 = Two's complement	OUTPUT_MODE<1:0> 11 = Do not use. Output is undefined 10 = LVDS, even bit first 01 = CMOS 00 = Output disabled		TEST_PATTERNS<2:0>			0x10
0x63	LVDS Output Load and Drive Current Control	FCB<3:0>				LVDS_LOAD	LVDS_IMODE<1:0>			0x01
0x64	Output Clock Phase Control when Decimation Filter is used	EN_PHDLY_DEC	DCLK_PHDLY_DEC<2:0>			FCB<3:0> = 0011				0x03

Legend: U = Unimplemented bit, read as ‘0’ FCB = Factory-controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x65	LVDS Output Polarity	POL_LVDS<7:0>								0x00
0x66	Digital Offset Correction — Lower Byte	DIG_OFFSET<7:0>								0x00
0x67	Digital Offset Correction — Upper Byte	DIG_OFFSET<15:8>								0x00
0x68	WCK and OVR Bit Control	FCB<5:2> = 0010				POL_WCK_OVR	EN_WCK_OVR	FCB<1:0>		0x24
						1 = Inverted	1 = Enabled	1 = Added	1 = Inverted	
0x6B	PLL Calibration	FCB<4:0>=0001					PLL_CALTRIG	FCB<1:0>=00		0x08
0x6D	PLL Output and Output Clock Phase	U<1:0>		EN_PLL_CLK	PLL_PHASE	PLL_PHDLY<3:0>				0x00
0x74	User-Defined Output Pattern A — Lower Byte	PATTERN A<3:0>				Do not use (Leave these bits as '0000')				0x00
0x75	User-Defined Output Pattern A — Upper Byte	PATTERN A<11:4>								0x00
0x76	User-Defined Output Pattern B — Lower Byte	PATTERN B<3:0>				Do not use (Leave these bits as '0000')				0x00
0x77	User-Defined Output Pattern B — Upper Byte	PATTERN B<11:4>								0x00
0x78	Noise-Shaping Requantizer Channel A Filter	NSR_RESET	NSRA<6:0>							0x00
0x79	Dual-Channel DSPP and Noise-Shaping Requantizer Channel B Filter	EN_DSPPDUAL	NSRB<6:0>							0x00
0x7A	FIRA0 Filter, FDR and NSR Control	U	FIR_A<0>	EN_FDR	FCB<0> = 0	EN_NSRB_11	EN_NSRB_12	EN_NSRA_11	EN_NSRA_12	0x00
0x7B	FIR A Filter (for Single, Dual)	FIR_A<8:1>								0x00
0x7C	FIR B Filter for Channel B	FIR_B<7:0>								0x00
0x7D	Auto-Scan Channel Order — Lower Byte	CH_ORDER<7:0>								0x78
0x7E	Auto-Scan Channel Order — Middle Byte	CH_ORDER<15:8>								0xAC
0x7F	Auto-Scan Channel Order — Upper Byte	CH_ORDER<23:16>								0x8E
0x80	Digital Down-Converter Control 1	HBFILTER_B	HBFILTER_A	EN_NCO	EN_AMPDITH	EN_PHSDITH	EN_LFSR	EN_DDC_FS/8	EN_DDC1	0x00
0x81	Digital Down-Converter Control 2	FDR_BAND	EN_DDC2	GAIN_HBF_DDC	SEL_FDR	SEL_DSPP	8CH_CW	GAIN_8CH<1:0>		0x00

Legend: U = Unimplemented bit, read as '0' FCB = Factory-controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x82	Numerically Controlled Oscillator (NCO) Tuning — Lower Byte	NCO_TUNE<7:0>								0x00
0x83	Numerically Controlled Oscillator (NCO) Tuning — Middle Lower Byte	NCO_TUNE<15:8>								0x00
0x84	Numerically Controlled Oscillator (NCO) Tuning — Middle Upper Byte	NCO_TUNE<23:16>								0x00
0x85	Numerically Controlled Oscillator (NCO) Tuning — Upper Byte	NCO_TUNE<31:24>								0x00
0x86	CH0 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH0_NCO_PHASE<7:0>								0x00
0x87	CH0 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH0_NCO_PHASE<15:8>								0x00
0x88	CH1 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH1_NCO_PHASE<7:0>								0x00
0x89	CH1 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH1_NCO_PHASE<15:8>								0x00
0x8A	CH2 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH2_NCO_PHASE<7:0>								0x00
0x8B	CH2 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH2_NCO_PHASE<15:8>								0x00
0x8C	CH3 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH3_NCO_PHASE<7:0>								0x00
0x8D	CH3 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH3_NCO_PHASE<15:8>								0x00
0x8E	CH4 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH4_NCO_PHASE<7:0>								0x00
0x8F	CH4 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH4_NCO_PHASE<15:8>								0x00

Legend: U = Unimplemented bit, read as ‘0’ FCB = Factory-controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown
Note 1: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0x90	CH5 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH5_NCO_PHASE<7:0>								0x00
0x91	CH5 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH5_NCO_PHASE<15:8>								0x00
0x92	CH6 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH6_NCO_PHASE<7:0>								0x00
0x93	CH6 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH6_NCO_PHASE<15:8>								0x00
0x94	CH7 NCO Phase Offset in CW or DDC Mode — Lower Byte	CH7_NCO_PHASE<7:0>								0x00
0x95	CH7 NCO Phase Offset in CW or DDC Mode — Upper Byte	CH7_NCO_PHASE<15:8>								0x00
0x96	CH0 Digital Gain	CH0_DIG_GAIN<7:0>								0x3C
0x97	CH1 Digital Gain	CH1_DIG_GAIN<7:0>								0x3C
0x98	CH2 Digital Gain	CH2_DIG_GAIN<7:0>								0x3C
0x99	CH3 Digital Gain	CH3_DIG_GAIN<7:0>								0x3C
0x9A	CH4 Digital Gain	CH4_DIG_GAIN<7:0>								0x3C
0x9B	CH5 Digital Gain	CH5_DIG_GAIN<7:0>								0x3C
0x9C	CH6 Digital Gain	CH6_DIG_GAIN<7:0>								0x3C
0x9D	CH7 Digital Gain	CH7_DIG_GAIN<7:0>								0x3C
0x9E	CH0 Digital Offset	CH0_DIG_OFFSET<7:0>								0x00
0x9F	CH1 Digital Offset	CH1_DIG_OFFSET<7:0>								0x00
0xA0	CH2 Digital Offset	CH2_DIG_OFFSET<7:0>								0x00
0xA1	CH3 Digital Offset	CH3_DIG_OFFSET<7:0>								0x00
0xA2	CH4 Digital Offset	CH4_DIG_OFFSET<7:0>								0x00
0xA3	CH5 Digital Offset	CH5_DIG_OFFSET<7:0>								0x00
0xA4	CH6 Digital Offset	CH6_DIG_OFFSET<7:0>								0x00
0xA5	CH7 Digital Offset	CH7_DIG_OFFSET<7:0>								0x00
0xA7	Digital Offset Weight Control	FCB<5:3> = `010`			DIG_OFFSET_WEIGHT<1:0>		FCB<2:0> = `111`			0x47
0xC0	Calibration Status Indication (read-only)	CAL_STAT	FCB<6:0> = `xxx-xxxx`							—

Legend: U = Unimplemented bit, read as ‘0’ FCB = Factory-controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown
Note 1: Read-only register. Preprogrammed at the factory for internal use.

TABLE 5-3: REGISTER MAP TABLE (CONTINUED)

Addr.	Register Name	Bits								Default Value
		b7	b6	b5	b4	b3	b2	b1	b0	
0xD1	PLL Calibration and Status Indication (read-only)	FCB<4:3> = xx		PLL_CAL_STAT	FCB<2:1> = xx		PLL_VCOL_STAT	PLL_VCOH_STAT	FCB<0> = x	—
0x15C	CHIP ID – Lower Byte[1] (read-only)	CHIP_ID<7:0>								—
0x15D	CHIP ID – Upper Byte[1] (read-only)	CHIP_ID<15:8>								—

Legend: U = Unimplemented bit, read as ‘0’ FCB = Factory-controlled bits. Do not program 1 = bit is set 0 = bit is cleared x = bit is unknown

Note 1: Read-only register. Preprogrammed at the factory for internal use.

REGISTER 5-1: ADDRESS 0X00 – SPI BIT ORDERING AND ADC MODE SELECTION (Note 1)

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
SHUTDOWN	LSB_FIRST	$\overline{\text{SOFT\_RESET}}$	STANDBY	STANDBY	$\overline{\text{SOFT\_RESET}}$	LSB_FIRST	SHUTDOWN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **SHUTDOWN:** Shutdown mode setting for power-saving (**Note 2**)
`1` = ADC in shutdown mode
`0` = Not in shutdown mode **(Default)**

bit 6 **LSB_FIRST:** Select SPI communication bit order
`1` = Start SPI communication with LSB first
`0` = Start SPI communication with MSB first **(Default)**

bit 5 **$\overline{\text{SOFT\_RESET}}$:** Soft Reset control bit (**Note 4**)
`1` = Not in Soft Reset mode **(Default)**
`0` = ADC in Soft Reset

bit 4 **STANDBY:** Send the device into a power-saving standby mode (**Note 3**)
`1` = ADC in Standby mode
`0` = Not in Standby mode **(Default)**

bit 3 **STANDBY:** Send the device into a power-saving standby mode (**Note 3**)
`1` = ADC in Standby mode
`0` = Not in Standby mode **(Default)**

bit 2 **$\overline{\text{SOFT\_RESET}}$:** Soft Reset control bit (**Note 4**)
`1` = Not in Soft Reset mode **(Default)**
`0` = ADC in Soft Reset

bit 1 **LSB_FIRST:** Select SPI communication bit order
`1` = Start SPI communication with LSB first
`0` = Start SPI communication with MSB first **(Default)**

bit 0 **SHUTDOWN:** Shutdown mode setting for power-saving (**Note 2**)
`1` = ADC in Shutdown mode
`0` = Not in Shutdown mode **(Default)**

Note 1: Upper and lower nibbles are mirrored, which makes the MSB or LSB-first mode interchangeable. The lower nibble (bit <3:0>) has a higher priority when the mirrored bits have different values.

2: During Shutdown mode, most of the internal circuits including the reference and clock are turned off except for the SPI interface. When exiting from shutdown (changing from ‘`1`’ to ‘`0`’), executing the device Soft Reset simultaneously is highly recommended for a fast recalibration of the ADC. The internal user registers are not affected.

3: During Standby mode, most of the internal circuits are turned off except for the reference, clock and SPI interface. When exiting from Standby mode (changing from ‘`1`’ to ‘`0`’) after an extended amount of time, executing Soft Reset simultaneously is highly recommended. The internal user registers are not affected.

4: This bit forces the device into the Soft Reset mode, which initializes the internal calibration registers to their initial default states. The user registers are not affected. When exiting the Soft Reset mode (changing from ‘`0`’ to ‘`1`’), the device performs an automatic device calibration. During the Soft Reset, the device has the following states:

- no ADC output
- no change in power-on condition of internal reference
- most of the internal clocks are not distributed

The power consumption of the digital section is negligible, but there is no change in the analog section.

REGISTER 5-2: ADDRESS 0X01 – NUMBER OF CHANNELS, INDEPENDENCY CONTROL OF OUTPUT DATA AND CLOCK DIVIDER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
EN_DATCLK_IND	FCB	SEL_NCH<2:0>			FCB<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EN_DATCLK_IND:** Enable data and clock divider independently (**Note 1**)
`1` = Enable
`0` = Disable **(Default)**

bit 6 **FCB:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 5-3 **SEL_NCH<2:0>:** Select the total number of input channels to be used (**Note 2**)
`111` = 7 inputs
`110` = 6 inputs
`101` = 5 inputs
`100` = 4 inputs
`011` = 3 inputs
`010` = 2 inputs
`001` = 1 input **(Default)**
`000` = 8 inputs

bit 2-0 **FCB<2:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

Note 1: EN_DATCLK_IND = `1` enables OUT_CLKRATE<3:0> settings in Address 0x02 (Register 5-3).

2: The total number of input channel varies with the device part number (P/N):
- Single/Dual/Quad-channel devices: SEL_NCH<2:0> bits are preprogammed at the factory.
- Octal-channel devices: SEL_NCH<2:0> bits are programmed by the user. See Addresses 0x7D – 0x7F (Registers 5-38 – 5-40) for selecting the input channel order.

REGISTER 5-3: ADDRESS 0X02 – OUTPUT DATA AND CLOCK RATE CONTROL (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUT_DATARATE<3:0>				OUT_CLKRATE<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **OUT_DATARATE<3:0>:** Output data rate control bits (**Note 2**)

`1111` = Output data is all 0s
`1110` = Output data is all 0s
`1101` = Output data is all 0s
`1100` = Internal test only
`1011` = Internal test only
`1010` = Internal test only
`1001` = Full speed divided by 512
`1000` = Full speed divided by 256
`0111` = Full speed divided by 128
`0110` = Full speed divided by 64
`0101` = Full speed divided by 32
`0100` = Full speed divided by 16
`0011` = Full speed divided by 8
`0010` = Full speed divided by 4
`0001` = Full speed divided by 2
`0000` = Full speed rate **(Default)**

bit 3-0 **OUT_CLKRATE<3:0>:** Output clock rate control bits (**Notes 3** and **4**)

`1111` = Full speed rate
`1110` = No clock output
`1101` = No clock output
`1100` = No clock output
`1011` = No clock output
`1010` = No clock output
`1001` = Full speed divided by 512
`1000` = Full speed divided by 256
`0111` = Full speed divided by 128
`0110` = Full speed divided by 64
`0101` = Full speed divided by 32
`0100` = Full speed divided by 16
`0011` = Full speed divided by 8
`0010` = Full speed divided by 4
`0001` = Full speed divided by 2
`0000` = No clock output **(Default)**

Note 1: This register should be used when the decimation filter selection option (see Addresses 0x7B and 0x7C – Registers 5-36 and 5-37) or digital down-conversion (DDC) option (see Address 0x80 – Register 5-41) is used in single or dual-channel mode.

2: `1100` – `1010`: Do not reprogram. These settings are used for the internal test only. If these bits are reprogrammed with different settings, the outputs will be in an undefined state.

3: Bits <3:0> become active if EN_DATCLK_IND = `1` in Address 0x01 (Register 5-2). This setting is only used with DDC mode. See Addresses 0x80 and 0x81 (Registers 5-41 and 5-42) for DDC settings.

4: When no clock output is selected (Bits `1110` – `1010`): clock output is not available at the DCLK+/DCLK- pins.

REGISTER 5-4: ADDRESS 0X04 – SPI SDO OUTPUT TIMING CONTROL

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SDO_TIME	FCB<6:0>						
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **SDO_TIME:** SPI SDO output timing control bit

`1` = SDO output at the falling edge of clock **(Default)**

`0` = SDO output at the rising edge of clock

bit 6-0 **FCB<6:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

REGISTER 5-5: ADDRESS 0X07 – OUTPUT RANDOMIZER AND WCK POLARITY CONTROL

R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
POL_WCK	EN_AUTOCAL_-TIMEDLY	FCB<4:0>					EN_OUT_RANDOM
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **POL_WCK:** WCK polarity control bit (**Note 1**)

`1` = Inverted

`0` = Not inverted **(Default)**

bit 6 **EN_AUTOCAL_TIMEDLY:** Auto-calibration starter time delay counter control bit (**Note 2**)

`1` = Enabled **(Default)**

`0` = Disabled

bit 5-1 **FCB<4:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 0 **EN_OUT_RANDOM:** Output randomizer control bit

`1` = Enabled: ADC data output is randomized

`0` = Disabled **(Default)**

Note 1: See Address 0x68 (Register 5-26) for WCK/OVR pair control.

2: This bit enables the AUTOCAL_TIMEDLY<7:0> settings. See Address 0x1E (Register 5-6).

REGISTER 5-6: ADDRESS 0X1E – AUTOCAL TIME DELAY CONTROL (Note 1)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
AUTOCAL_TIMEDLY<7:0>							
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7-0 **AUTOCAL_TIMEDLY<7:0>:** Auto-calibration start time delay control bits

`1111-1111` = Maximum value
•
•
•
`1000-0000` = **(Default)**
•
•
•
`0000-0000` = Minimum value

Note 1: EN_AUTOCAL_TIMEDLY in Address 0x07 (Register 5-5) enables this register setting. This register controls the time delay before the auto-calibration starts. The value increases linearly with the bit settings, from minimum to maximum values.

REGISTER 5-7: ADDRESS 0X52 – DLL CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
EN_DUTY	DLL_PHDLY<2:0>			EN_DCLK	EN_DLL	EN_CLK	$\overline{\text{RESET\_DLL}}$
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **EN_DUTY:** Enable DLL circuit for duty cycle correction (DCC) of input clock (**Note 1**)

`1` = Correction is ON
`0` = Correction is OFF **(Default)**

bit 6-4 **DLL_PHDLY<2:0>:** Select the phase delay of the clock output (**Note 2**)

`111` = 360°
`110` = 315°
`101` = 270°
`100` = 225°
`011` = 180°
`010` = 135°
`001` = 90°
`000` = 45° **(Default)**

Note 1: Enable the DLL circuitry for the duty cycle correction. Analog clock output: Rising edge is unaffected and only falling edge is modified. The duty cycle correction will significantly affect the SNR performance.

2: **Phase of output data:**

- In CMOS output, the data transition occurs at the rising edge of the DCLK+.
- In DDR LVDS output, the data transition occurs at both rising and falling edges of the DCLK+.

3: DLL must be reset if clock is removed or clock frequency is changed significantly. DLL resets automatically during the power-up process. The DLL reset control procedure: set this bit to ‘`0`’ (reset) and then to ‘`1`’.

REGISTER 5-7: ADDRESS 0X52 – DLL CONTROL (CONTINUED)

bit 3	**EN_DCLK:** Enable digital clock to the circuit `1` = Enabled **(Default)** `0` = Disabled: Digital clock is turned off, therefore ADC output is not available.
bit 2	**EN_DLL:** Enable DLL circuitry to provide a selectable phase clock to digital output clock. `1` = Enabled `0` = Disabled. Phase selection of digital output is not available **(Default)**
bit 1	**EN_CLK:** Enable internal clock circuitry `1` = Enabled **(Default)** `0` = Disabled. No clock is available to the internal circuits, ADC output is not available.
bit 0	**$\overline{\text{RESET\_DLL}}$:** DLL circuit reset control (**Note 3**) `1` = DLL is active `0` = DLL circuit is held in reset **(Default)**

Note 1: Enable the DLL circuitry for the duty cycle correction. Analog clock output: Rising edge is unaffected and only falling edge is modified. The duty cycle correction will significantly affect the SNR performance.

2: Phase of output data:

- In CMOS output, the data transition occurs at the rising edge of the DCLK+.
- In DDR LVDS output, the data transition occurs at both rising and falling edges of the DCLK+.

3: DLL must be reset if clock is removed or clock frequency is changed significantly. DLL resets automatically during the power-up process. The DLL reset control procedure: set this bit to ‘`0`’ (reset) and then to ‘`1`’.

REGISTER 5-8: ADDRESS 0X53 – CLOCK SOURCE SELECTION

R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FCB<6:4>			CLK_SOURCE	FCB<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5	**FCB<6:4>:** Factory-controlled bits. This is not for the user. Do not change the default settings.
bit 4	**CLK_SOURCE:** Select internal timing source `1` = PLL output is selected as timing source `0` = External clock input is selected as timing source (PLL is not used) **(Default)**
bit 3-0	**FCB<3:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

REGISTER 5-9: ADDRESS 0X54 – PLL REFERENCE DIVISOR

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLL_REFDIV<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PLL_REFDIV<7:0>:** PLL Reference clock divisor control bits (**Note 1**)

`1111-1111` = PLL reference divided by 255 (if PLL_REFDIV<9:8> = `00`)
`1111-1110` = PLL reference divided by 254 (if PLL_REFDIV<9:8> = `00`)
•
•
•
`0000-0011` = PLL reference divided by 3 (if PLL_REFDIV<9:8> = `00`)
`0000-0010` = **Do not use (No effect)**
`0000-0001` = PLL reference divided by 1 (if PLL_REFDIV<9:8> = `00`)
`0000-0000` = PLL reference not divided (if PLL_REFDIV<9:8> = `00`) **(Default)**

Note 1: PLL_REFDIV is a 10-bit wide setting. See Address 0x55 (Register 5-10) for the upper two bits and **Table 4-4** for PLL_REFDIV<9:0> bit settings. This setting controls the clock division ratio of the PLL reference clock (external clock input at the clock input pin) before the PLL phase-frequency detector circuitry. Note that the divider value of 2 is not supported. EN_PLL_REFDIV in Address 0x59 (Register 5-14) must be set.

REGISTER 5-10: ADDRESS 0X55 – PLL OUTPUT AND REFERENCE DIVISOR

R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
PLL_OUTDIV<3:0>				U<1:0>		PLL_REFDIV<9:8>	
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **PLL_OUTDIV<3:0>:** PLL output divisor control bits (**Note 1**)

`1111` = PLL output divided by 15
`1110` = PLL output divided by 14
•
•
•
`0100` = PLL output divided by 4 **(Default)**
`0011` = PLL output divided by 3
`0010` = PLL output divided by 2
`0001` = PLL output divided by 1
`0000` = PLL output not divided

bit 3-2 **U<1:0>:** Unimplemented. No effect.

bit 1-0 **PLL_REFDIV<9:8>:** Upper two MSB bits of PLL_REFDIV<9:0> (**Note 2**)

`00` = See Table 5-4 **(Default)**

Note 1: PLL_OUTDIV<3:0> controls the PLL output clock divider: VCO output is divided by the PLL_OUTDIV<3:0> setting.

2: See Address 0x54 (Register 5-9) and Table 5-4 for PLL_REFDIV<9:0> bit settings. EN_PLL_REFDIV in Address 0x59 (Register 5-14) must be set.

TABLE 5-4: EXAMPLE – PLL REFERENCE DIVISOR BIT SETTINGS VS. PLL REFERENCE INPUT FREQUENCY

PLL_REFDIV<9:0>	PLL Reference Frequency
`11-1111-1111`	Reference frequency divided by 1023
`11-1111-1110`	Reference frequency divided by 1022
`---`	`---`
`00-0000-0011`	Reference frequency divided by 3
`00-0000-0010`	Do not use (Not supported)
`00-0000-0001`	Reference frequency divided by 1
`00-0000-0000`	Reference frequency divided by 1

REGISTER 5-11: ADDRESS 0X56 – PLL PRESCALER (LSB)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLL_PRE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PLL_PRE<7:0>:** PLL prescaler selection (**Note 1**)

`1111-1111` = VCO clock divided by 255 (if PLL_PRE<11:8> = `0000`)
•
•
•
`0111-1000` = VCO clock divided by 120 (if PLL_PRE<11:8> = `0000`) **(Default)**
•
•
•
`0000-0010` = VCO clock divided by 2 (if PLL_PRE<11:8> = `0000`)
`0000-0001` = VCO clock divided by 1 (if PLL_PRE<11:8> = `0000`)
`0000-0000` = VCO clock not divided (if PLL_PRE<11:8> = `00000`)

Note 1: PLL_PRE is a 12-bit wide setting. The upper four bits (PLL_PRE<11:8>) are defined in Address 0x57. See **Table 4-4** for the PLL_PRE<11:0> bit settings. The PLL Prescaler is used to divide down the VCO output clock in the PLL phase-frequency detector loop circuit.

REGISTER 5-12: ADDRESS 0X57 – PLL PRESCALER (MSB)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FCB<3:0>				PLL_PRE<11:8>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<3:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 3-0 **PLL_PRE<11:8>:** PLL prescaler selection (**Note 1**)

`1111` = $2^{12} – 1$ (maximum), if PLL_PRE<7:0> = 0xFF
•
•
•
`0000` = **(Default)**

Note 1: PLL_PRE is a 12-bit wide setting. See the lower eight bit settings (PLL_PRE<7:0>) in Address 0x56 (Register 5-11). See **Table 4-4** for the PLL_PRE<11:0> bit settings for PLL feedback frequency.

TABLE 5-5: EXAMPLE – PLL PRESCALER BIT SETTINGS AND PLL FEEDBACK FREQUENCY

PLL_PRE<11:0>	PLL Feedback Frequency
`1111-1111-1111`	VCO clock divided by 4095 (2^{12} - 1)
`1111-1111-1110`	VCO clock divided by 4094 (2^{12} - 2)
`---`	`---`
`0000-0000-0011`	VCO clock divided by 3
`0000-0000-0010`	VCO clock divided by 2
`0000-0000-0001`	VCO clock divided by 1
`0000-0000-0000`	VCO clock divided by 1

REGISTER 5-13: ADDRESS 0X58 – PLL CHARGE PUMP

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
FCB<2:0>:			PLL_BIAS	PLL_CHAGPUMP<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **FCB<2:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 5 **PLL_BIAS:** PLL charge pump bias source selection bit (**Note 1**)

`1` = Self-biasing coming from AV_{DD}.
`0` = Bandgap voltage from the reference generator (1.2V) **(Default)**

bit 4-0 **PLL_CHAGPUMP<3:0>:** PLL charge pump bias current control bits (**Note 2**)

`1111` = Maximum current
•
•
•
`0010` = **(Default)**
•
•
•
`0000` = Minimum current

Note 1: This bit can be controlled by the factory.

2: PLL_CHAGPUMP<3:0> bits should be set based on the phase detector comparison frequency. The bias current amplitude increases linearly with increasing the bit setting values. The increase is from approximately 25 µA to 375 µA, 25 µA per step. See **Section 4.7.2 “PLL Output Frequency and Control Parameters”** for more details on the PLL block.

REGISTER 5-14: ADDRESS 0X59 – PLL ENABLE CONTROL 1

U-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	FCB<4:3>		EN_PLL_REFDIV	FCB<2:1>		EN_PLL	FCB<0>
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<4:3>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 4 **EN_PLL_REFDIV:** Enable PLL Reference Divider (PLL_REFDIV<9:0>).

`1` = Enable PLL_REFDIV<9:0> register
`0` = Reference divider is bypassed **(Default)**

bit 3-2 **FCB<2:1>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 1 **EN_PLL:** Master enable bit for PLL circuit.

`1` = Enable PLL circuit
`0` = Disable PLL circuit **(Default)**

bit 0 **FCB<0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

REGISTER 5-15: ADDRESS 0X5A – PLL LOOP FILTER RESISTOR

U-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_RES<4:0>				
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’

-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.

bit 4-0 **PLL_RES<4:0>:** Resistor value selection bits for PLL loop filter (**Note 1**)

`11111` = Maximum value
•
•
•
`00111`= **(Default)**
•
•
•
`00000` = Minimum value

Note 1: PLL_RES<4:0> bits should be set based on the phase detector comparison frequency. The resistor value increases linearly with the bit settings, from minimum to maximum values. See the PLL loop filter section in **Section 4.7 “ADC Clock Selection and PLL Output Frequency Control”**.

REGISTER 5-16: ADDRESS 0X5B – PLL LOOP FILTER CAP3

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP3<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**Unimplemented:** Not used.
bit 6-5	**FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.
bit 4-0	**PLL_CAP3<4:0>:** Capacitor 3 value selection bits for PLL loop filter (**Note 1**) `11111` = Maximum value • • • `01111`= **(Default)** • • • `00000` = Minimum value

Note 1: This capacitor is in series with the shunt resistor, which is set by PLL_RES<4:0> bits. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-17: ADDRESS 0X5C – PLL LOOP FILTER CAP1

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP1<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7	**Unimplemented:** Not used.
bit 6-5	**FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.
bit 4-0	**PLL_CAP1<4:0>:** Capacitor 1 value selection bits for PLL loop filter (**Note 1**) `11111` = Maximum value • • • `00111`= **(Default)** • • • `00000` = Minimum value

Note 1: This capacitor is located between the charge pump output and ground and in parallel with the shunt resistor which is defined by the PLL_RES<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-18: ADDRESS 0X5D – PLL LOOP FILTER CAP2

U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
—	FCB<1:0>		PLL_CAP2<4:0>				
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6-5 **FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.

bit 4-0 **PLL_CAP2<4:0>:** Capacitor 2 value selection bits for PLL loop filter (**Note 1**)

`11111` = Maximum value
•
•
•
`00111`= **(Default)**
•
•
•
`00000` = Minimum value

Note 1: This capacitor is located between the charge pump output and ground and in parallel with CAP1 which is defined by the PLL_CAP1<4:0>. The capacitor value increases linearly with the bit settings, from minimum to maximum values. This setting should be set based on the phase detector comparison frequency.

REGISTER 5-19: ADDRESS 0X5F – PLL ENABLE CONTROL 2 (Note 1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1
FCB<5:2>				EN_PLL_OUT	EN_PLL_BIAS	FCB<1:0>	
bit 7							bit 0

Legend:
R = Readable bit W = Writable bit U = Unimplemented bit, read as ‘0’
-n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 7-4 **FCB<5:2>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

bit 3 **EN_PLL_OUT:** Enable PLL output.
`1` = Enable PLL output
`0` = Disable PLL output **(Default)**

bit 2 **EN_PLL_BIAS:** Enable PLL bias
`1` = Enable PLL bias
`0` = Disable PLL bias **(Default)**

bit 1-0 **FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not change the default settings.

Note 1: To enable PLL output, EN_PLL_OUT, EN_PLL_BIAS and EN_PLL in Address 0x59 (Register 5-14) must be set.

REGISTER 5-20: ADDRESS 0X62 – OUTPUT DATA FORMAT AND OUTPUT TEST PATTERN

U-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	FCB	DATA_FORMAT	OUTPUT_MODE<1:0>		TEST_PATTERNS<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used.

bit 6 **FCB:** Factory-controlled bit. This is not for the user. Do not program.

bit 5 **DATA_FORMAT**: Output data format selection

`1` = Offset binary (unsigned)
`0` = Two’s complement **(Default)**

bit 4-3 **OUTPUT_MODE<1:0>**: Output mode selection (**Note 1**)

`11` = Do not use. Output is undefined
`10` = Select DDR LVDS output mode with even bit first (**Note 2**) **(Default)**
`01` = Select CMOS output mode
`00` = Output disabled

bit 2-0 **TEST_PATTERNS<2:0>**: Test output data pattern selection (**Note 3**)

`111` = Output data is pseudo-random number (PN) sequence (**Note 4**)
`110` = Sync Pattern for LVDS output
Output: '`11111111 0000`'
`101` = Alternating Sequence for LVDS mode
Output: ‘`01010101 1010`’
`100` = Alternating Sequence for CMOS mode
Output: ‘`11111111 1111`’ alternating with ‘`00000000 0000`’
`011` = Alternating Sequence for CMOS
Output: ‘`01010101 0101`’ alternating with ‘`10101010 1010`’
`010` = Ramp Pattern: Output (Q0) is incremented by1 LSB per 64 clock cycles (**Note 5**)
`001` = Double Custom Patterns
Output: Alternating custom pattern A (see Addresses 0X74 - 0X75 – Registers 5-29 – 5-30) and custom pattern B (see Address 0X76 - 0X77 – Registers 5-31 – 5-32) (**Note 6**)
`000` = Normal Operation. Output: ADC data **(Default)**

Note 1: See Figures 2-1 – 2-2 for the timing diagrams.

2: Rising edge: Q10, Q8, Q6, Q4, Q2, Q0.
Falling edge: Q11, Q9, Q7, Q5, Q3, Q1.

3: See **Section 4.15 “Output Test Patterns”** for more details.
(a) In LVDS mode: only the active pins (per register settings) are active. Inactive output pins are High Z state.
(b) In CMOS mode: all data output pins (Q11-Q0), output test pins (TP), OVR and WCK pins are active, even if they are disabled by register settings.
Since the output test pins (TP) can toggle during this test, the output test pins can draw extra current if they are connected to the supply pin or ground. To avoid the extra current draws, always leave the TP pins floating (not connected).

4: Pseudo-random number (PN) code is generated by the linear feedback shift register (LFSR). See **Section 4.15.1 “Pseudo-Random Number (PN) Sequence Output”** for more details.

5: OVR and WCK bits are incremented by 1 per 2^{19} and 2^{18} clock cycles, respectively.

6: Pattern A<11:0> and B<11:0> are applied to Q<11:0>. Q11 = OVR, Q10 = WCK.

REGISTER 5-21: ADDRESS 0X63 – LVDS OUTPUT LOAD AND DRIVER CURRENT CONTROL

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
FCB<3:0>				LVDS_LOAD	LVDS_IMODE		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<3:0>:** Factory-controlled bits. This is not for the user. Do not program.

bit 3 **LVDS_LOAD**: Internal LVDS load termination

`1` = Enable internal load termination
`0` = Disable internal load termination **(Default)**

bit 2-0 **LVDS_IMODE<2:0>**: LVDS driver current control bits

`111` = 7.2 mA
`011` = 5.4 mA
`001` = 3.5 mA **(Default)**
`000` = 1.8 mA
Do not use the following settings (Note 1):
`110, 101, 100, 010`

Note 1: Do not use these settings. These settings can result in unknown outputs currents.

REGISTER 5-22: ADDRESS 0X64 – OUTPUT CLOCK PHASE CONTROL WHEN DECIMATION FILTER IS USED

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
EN_PHDLY_DEC	DCLK_PHDLY_DEC<2:0>			FCB<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EN_PHDLY_DEC:** Enable digital output clock phase delay control when decimation filter is used.
`1` = DCLK_PHDLY_DEC<2:0> setting is enabled (**Note 1**)
`0` = DCLK_PHDLY_DEC<2:0> setting is disabled **(Default)**

bit 6-4 **DCLK_PHDLY_DEC<2:0>**: Digital output clock phase delay control when decimation filter is used (**Note 2**)
`111` = 315° phase-shifted (**Note 3**)
`110` = 270° phase-shifted
`101` = 225° phase-shifted (**Note 3**)
`100` = 180° phase-shifted
`011` = 135° phase-shifted (**Note 3**)
`010` = 90° phase-shifted
`001` = 45° phase-shifted (**Note 3**)
`000` = In-Phase **(Default)**

bit 3-0 **FCB<3:0>:** Factory-controlled bits. This is not for the user. Do not program.

Note 1: This feature is only used in conjunction with the decimation filter options where the core clock frequency is faster than the output clock frequency.

2: This bit is enabled only if EN_PHDLY_DEC = `1`. These bits are used when the divided clocks are used. See OUT_CLKRATE<3:0> bits in Address 0x02 (Register 5-3). When the full speed clock is selected, the same feature is provided by the DLL phases. See Address 0x52 (Register 5-7).

3: Only available when the decimation filter setting is greater than 2. When FIR_A/B <8:1> = `0`’s (default) and FIR_A<6> = `0`, only four phases are available (0, 90, 180, 270). See Addresses 0x7A, 0x7B and 0x7C (Registers 5-35 – 5-37). See address 0x6D and 0x52 DCLK (Registers 5-7 and 5-28) phase shift for other modes.

REGISTER 5-23: ADDRESS 0X65 – LVDS OUTPUT POLARITY

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POL_LVDS<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **POL_LVDS<7:0>:** Control polarity of LVDS data pairs
`1111-1111` = Invert all LVDS pairs
`1111-1110` = Invert all LVDS pairs except the LSB pair
•
•
•
`1000-0000` = Invert MSB LVDS pair
•
•
•
`0000-0001` = Invert LSB LVDS pair
`0000-0000` = No inversion of LVDS bit pairs (**Default)**

REGISTER 5-24: ADDRESS 0X66 – DIGITAL OFFSET CORRECTION (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIG_OFFSET <7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_OFFSET <7:0>:** Lower byte of DIG_OFFSET<15:0> (**Note 1**)

`0000-0000` = 0 LSB **(Default)**

Note 1: Offset is added to the ADC output. Setting is two’s complement using two combined registers (16 bits).

- Step size of each bit setting: 0.125 LSB
- Setting range: (-2^{15} to $2^{15} – 1$) x 0.125 LSB or (-32768 to +32767) x 0.125 LSB

REGISTER 5-25: ADDRESS 0X67 – DIGITAL OFFSET CORRECTION (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIG_OFFSET<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **DIG_OFFSET <15:8>:** Upper byte of DIG_OFFSET<15:0> (**Note 1**)

`0000-0000` = **Default**

Note 1: Offset is added to the ADC output. Setting is two’s complement using two combined registers (16 bits).

- Step size of each bit setting: 0.125 LSB
- Setting range: (-2^{15} to $2^{15} – 1$) x 0.125 LSB or (-32768 to +32767) x 0.125 LSB

REGISTER 5-26: ADDRESS 0X68 – WCK AND OVR BIT CONTROL

R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
FCB<5:2>				POL_WCK_OVR	EN_WCK_OVR	FCB<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **FCB<5:2>:** Factory-controlled bits. This is not for the user. Do not program.

bit 3 **POL_WCK_OVR**: Polarity control for WCK and OVR bit pair in LVDS mode

`1` = Inverted
`0` = Not inverted **(Default)**

bit 2 **EN_WCK_OVR**: Enable WCK and OVR output bit pair

`1` = Enabled **(Default)**
`0` = Disabled

bit 1-0 **FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.

REGISTER 5-27: ADDRESS 0X6B – PLL CALIBRATION

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
FCB<6:2>					PLL_CALTRIG	FCB<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **FCB<6:2>:** Factory-controlled bits. This is not for the user. Do not program.

bit 3 **PLL_CALTRIG**: Manually force recalibration of the PLL at the state of bit transition (**Note 1**)

Toggle from ‘`1`’ to ‘`0`’ or from ‘`0`’ to ‘`1`’ = Start PLL calibration

bit 2-0 **FCB<1:0>:** Factory-controlled bits. This is not for the user. Do not program.

Note 1: PLL calibration status is observed by the PLL calibration status bit PLL_CAL in Address 0xD1 (Register 5-81). PLL should be recalibrated following a change in input frequency or PLL configuration registers (Address 0x54 - 0x57, Registers 5-9 – 5-12).

REGISTER 5-28: ADDRESS 0X6D – PLL OUTPUT AND OUTPUT CLOCK PHASE (Note 1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—		EN_PLL_CLK	PLL_PHASE	PLL_PHDLY<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-3 **Unimplemented:** Not used

bit 3 **EN_PLL_CLK:** Enable PLL output clock
`1` = PLL output clock is enabled to the ADC core
`0` = PLL clock output is disabled **(Default)**

bit 2-0 **PLL_PHASE:** Select PLL phase for internal delay line
`1` = Falling Edge
`0` = Rising Edge **(Default)**

bit 2-0 **PLL_PHDLY<3:0>:** Output clock is delayed by the number of VCO clock cycles from the nominal PLL output (**Note 2**)
`1111` = Delay of 15 cycles
`1110` = Delay of 14 cycles
•
•
•
`0001` = Delay of one cycle
`0000` = No delay **(Default)**

Note 1: This register has effect only when the PLL clock is selected by the CLK_SOURCE bit in Address 0x53 (Register 5-8) and PLL circuit is enabled by EN_PLL bit in Address 0x59 (Register 5-14).

2: This bit setting enables the output clock phase delay. This phase delay control option is applicable when PLL is used as the clock source and the decimation is not used.

REGISTER 5-29: ADDRESS 0X74 – USER-DEFINED OUTPUT PATTERN A (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_A<3:0>				**Do not use (Leave these bits as ‘`0000`’)**			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **PATTERN_A<3:0>:** Lower nibble of PATTERN_A<11:0> (**Note 1**)

bit 3-0 **Do not use:** Leave these bits to default settings (‘`0000`’) (**Note 2**)

Note 1: See PATTERN_A<11:4> in Address 0x75 (Register 5-30) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

2: The output from these bit settings is on “Unused Output Pattern Test Pins”, which are recommended to be not connected to the host device. Therefore, the effect of these bit settings is not monitored. Leave these bits as default settings (‘`0000`’) all the time.

REGISTER 5-30: ADDRESS 0X75 – USER-DEFINED OUTPUT PATTERN A (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_A<11:4>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PATTERN_A<11:4>:** Upper byte of PATTERN_A<11:0> (**Note 1**)

Note 1: See PATTERN_A<3:0> in Address 0x74 (Register 5-29) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

REGISTER 5-31: ADDRESS 0X76 – USER-DEFINED OUTPUT PATTERN B (LOWER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_B<3:0>				**Do not use (Leave these bits as ‘`0000`’)**			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **PATTERN_B<3:0>:** Lower nibble of PATTERN_B<11:0> (**Note 1**)

bit 3-0 **Do not use:** Leave these bits to default settings (‘`0000`’) (**Note 2**)

Note 1: See PATTERN_B<11:4> in Address 0x77 (Register 5-32) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

2: The output from these bit settings are on “Unused Output Pattern Test Pins”, which are recommended to be not connected to the host device. Therefore, the effect of these bit settings is not monitored. Leave these bits as default settings (‘`0000`’) all the time.

REGISTER 5-32: ADDRESS 0X77 – USER-DEFINED OUTPUT PATTERN B (UPPER BYTE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PATTERN_B<11:4>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **PATTERN_B<11:4>:** Upper byte of PATTERN_B<11:0> (**Note 1**)

Note 1: See PATTERN_B<3:0> in Address 0x76 (Register 5-31) and TEST_PATTERNS<2:0> in Address 0x62 (Register 5-20).

REGISTER 5-33: ADDRESS 0X78 – NOISE-SHAPING REQUANTIZER RESET CONTROL AND CHANNEL A FILTER (NSRA) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
NSR_RESET	NSRA<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **NSR_RESET:** Toggle of this bit causes a reset of the NSRA and NSRB state.
- Toggle from ‘`1`’ to ‘`0`’ or from ‘`0`’ to ‘`1`’ = Reset of NSRA and NSRB (**Note 2**)
- Otherwise = No effect **(Default)**

bit 6-0 **NSRA<6:0>:** NSRA filter settings. See Tables 4-10 to 4-12 for the NSR filter settings (**Note 3**)
`000-0000` = **(Default)**

Note 1: This register is used for single and dual-channel modes only.
2: The NSR filter will be also automatically reset if the filter setting is changed.
3: In dual-channel mode, NSRA<6:0> is used for channel A.

REGISTER 5-34: ADDRESS 0X79 – DUAL-CH DSPP AND NOISE-SHAPING REQUANTIZER CHANNEL B FILTER (NSRB) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
EN_DSPPDUAL	NSRB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **EN_DSPPDUAL:** Enable digital post-processing functions for dual-channel operations
`1` = Dual-channel DSPP is enabled
`0` = Disabled **(Default)**

bit 6-0 **NSRB<6:0>:** NSRB filter settings. See Tables 4-10 to 4-12 for the NSR filter settings (**Note 2**)
`000-0000` = **(Default)**

Note 1: This register is used for single and dual-channel modes only.
2: In dual-channel mode, NSRB<6:0> is used for channel B.

REGISTER 5-35: ADDRESS 0X7A – FIRA0 FILTER, FDR AND NSR CONTROL (Note 1)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FIR_A<0>	EN_FDR	FCB	EN_NSRB_11	EN_NSRB_12	EN_NSRA_11	EN_NSRA_12
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Not used

bit 6 **FIR_A<0>:** Enable the first 2x decimation (Stage 1A in FIR A) in single-channel mode **(Note 2)**

`1` = Enabled
`0` = Disabled **(Default)**

bit 5 **EN_FDR:** Fractional Delay Recovery (FDR) control bit

`1` = Enabled (with delay of 59 samples)
`0` = Disabled **(Default)**

bit 4 **FCB:** Factory-controlled bits. This is not for the user. Do not program.

bit 3 **EN_NSRB_11:** Enable 11-bit noise-shaping requantizer for Channel B

`1` = Enabled
`0` = Disabled **(Default)**

bit 2 **EN_NSRB_12:** Enable 12-bit noise-shaping requantizer for Channel B

`1` = Enabled
`0` = Disabled **(Default)**

bit 1 **EN_NSRA_11:** Enable 11-bit noise-shaping requantizer for Channel A

`1` = Enabled
`0` = Disabled **(Default)**

bit 0 **EN_NSRA_12:** Enable 12-bit noise-shaping requantizer for Channel A

`1` = Enabled
`0` = Disabled **(Default)**

Note 1: This register is used only for single and dual-channel modes.

2: This is LSB of FIR_A filter settings. For the first 2x decimation, set FIR_A<0> = `1` for single-channel operation and FIR_A<0> = `0` for dual-channel operation. See Address 0x7B (Register 5-36) for FIR_A<8:1> settings.

REGISTER 5-36: ADDRESS 0X7B – FIR A FILTER (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIR_A<8:1>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **FIR_A<8:0>:** Decimation Filter FIR A settings for Channel A (or I) (**Note 2**, **Note 5**)

Single-Channel Mode: (Note 3)

`1-1111-1111` = Enabled stage 1 - 9 filters (decimation rate: 512)
`0-1111-1111` = Enabled stage 1 - 8 filters
`0-0111-1111` = Enabled stage 1 - 7 filters
`0-0011-1111` = Enabled stage 1 - 6 filters
`0-0001-1111` = Enabled stage 1 - 5 filters
`0-0000-1111` = Enabled stage 1 - 4 filters
`0-0000-0111` = Enabled stage 1 - 3 filters (decimation rate = 8)
`0-0000-0011` = Enabled stage 1 - 2 filters (decimation rate = 4)
`0-0000-0001` = Enabled stage 1 filter (decimation rate = 2)
`0-0000-0000` = Disabled all FIR A filters. **(Default)**

Dual-Channel Mode: (Note 4)

`1-1111-1110` = Enabled stage 2 - 9 filters (decimation rate: 256)
`0-1111-1110` = Enabled stage 2 - 8 filters
`0-0111-1110` = Enabled stage 2 - 7 filters
`0-0011-1110` = Enabled stage 2 - 6 filters
`0-0001-1110` = Enabled stage 2 - 5 filters
`0-0000-1110` = Enabled stage 2 - 4 filters
`0-0000-0110` = Enabled stage 2 - 3 filters
`0-0000-0010` = Enabled stage 2 filter (decimation rate = 2)
`0-0000-0000` = Disabled all FIR A filters. **(Default)**

Note 1: This register is used only for single and dual-channel modes. The register values are thermometer-encoded.

2: SNR is improved by approximately 2.5 dB per each filter stage, but output data rate is reduced by a factor of 2 per stage. The data and clock rates in Address 0X02 (Register 5-3) need to be updated accordingly when this register is updated. Address 0x64 (Register 5-22) setting is also affected. The maximum decimation factor is 512 for the single-channel mode and 256 for the dual-channel mode.

3: In single-channel mode, the 1st stage filter is selected by FIR_A<0> = `1` in Address 0x7A (Register 5-35).

4: In dual-channel mode, the 1st stage filter is disabled by setting FIR_A<0> = `0` in Address 0x7A (Register 5-35).

5: FIR_A<0> in Address 0x7A is LSB of FIR_A setting. See **Section 4.8.3 “Decimation Filters”** for the decimation filter.

REGISTER 5-37: ADDRESS 0X7C – FIR B FILTER (Note 1, Note 2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FIR_B<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **FIR_B<7:0>:**Decimation Filter FIR B settings for Channel B (or Q) (**Note 3**, **Note 4**)

`1111-1111` = Enabled stage 2 - 9 filters (decimation rate = 256)
`0111-1111` = Enabled stage 2 - 8 filters
`0011-1111` = Enabled stage 2 - 7 filters
`0001-1111` = Enabled stage 2 - 6 filters
`0000-1111` = Enabled stage 2 - 5 filters
`0000-0111` = Enabled stage 2 - 4 filters
`0000-0011` = Enabled stage 2 - 3 filters
`0000-0001` = Enabled stage 2 filter (decimation rate = 2)
`0000-0000` = Disabled all FIR B Filters. **(Default)**

Note 1: This register is used for the dual-channel mode only. The register values are thermometer-encoded an can be preprogrammed at the factory.

2: EN_DSPPDUAL bit in Address 0x79 (Register 5-34) must be set when using this register.

3: SNR is improved by approximately 2.5 dB per each filter stage, but output data rate is reduced by a factor of 2 per stage. The maximum decimation factor for the dual-channel mode is 256. The data and clock rates in Address 0X02 (Register 5-3) need to be updated accordingly when this register is updated. Address 0x64 (Register 5-22) setting is also affected.

4: See **Section 4.8.3 “Decimation Filters”**for the decimation filter.

REGISTER 5-38: ADDRESS 0X7D – AUTO-SCAN CHANNEL ORDER (LOWER BYTE)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0
CH_ORDER<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH_ORDER<7:0>:** Lower byte of CH_ORDER<31:0> (**Note 1**)

`0111-1000` = **Default**

Note 1: See Table 4-1 for the channel order selection. See SEL_NCH<2:0> in Address 0x01 (Register 5-2) for the number of channels to be selected.

REGISTER 5-39: ADDRESS 0X7E – AUTO-SCAN CHANNEL ORDER (MIDDLE BYTE)

R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
CH_ORDER<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH_ORDER<15:8>:** Middle byte of CH_ORDER<31:0> (**Note 1**)
`1010-1100` = **Default**

Note 1: See Table 4-1 for the channel order selection. See SEL_NCH<2:0> in Address 0x01 (Register 5-2) for the number of channels to be selected.

REGISTER 5-40: ADDRESS 0X7F – AUTO-SCAN CHANNEL ORDER (UPPER BYTE)

R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-0
CH_ORDER<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH_ORDER<23:16>:** Upper byte of CH_ORDER<31:0> (**Note 1**)
`1000-1110` = **Default**

Note 1: See Table 4-1 for the channel order selection. See SEL_NCH<2:0> in Address 0x01 (Register 5-2) for the number of channels to be selected.

REGISTER 5-41: ADDRESS 0X80 – DIGITAL DOWN-CONVERTER CONTROL 1 (MCP37D11-200) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HBFILTER_B	HBFILTER_A	EN_NCO	EN_AMPDITH	EN_PHSDITH	EN_LFSR	EN_DDC_FS/8	EN_DDC1
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **HBFILTER_B:** Select half-bandwidth filter at DDC output of channel B in dual-channel mode **(Note 2)**

1 = Select High-Pass filter at DDC output
0 = Select Low-Pass filter at DDC output **(Default)**

bit 6 **HBFILTER_A:** Select half-bandwidth filter at DDC output of channel A **(Note 2)**

1 = Select High-Pass filter at DDC output
0 = Select Low-Pass filter at DDC output **(Default)**

bit 5 **EN_NCO:** Enable NCO of DDC1

1 = Enabled
0 = Disabled **(Default)**

bit 4 **EN_AMPDITH:** Enable amplitude dithering for NCO **(Note 3, Note 4)**

1 = Enabled
0 = Disabled **(Default)**

bit 3 **EN_PHSDITH:** Enable phase dithering for NCO **(Note 3, Note 4)**

1 = Enabled
0 = Disabled **(Default)**

bit 2 **EN_LFSR:** Enable linear feedback shift register (LFSR) for amplitude and phase dithering for NCO

1 = Enabled
0 = Disabled **(Default)**

bit 1 **EN_DDC_FS/8:** Enable NCO for the DDC2 to center the DDC output signal to be around f_S/8/DER **(Note 5)**

1 = Enabled
0 = Disabled **(Default)**

bit 0 **EN_DDC1:** Enable digital down converter 1 (DDC1)

1 = Enabled **(Note 6)**
0 = Disabled **(Default)**

Note 1: This register is used for single, dual and octal-channel modes when the CW feature is enabled (8CH_CW = 1). This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: This filter includes a decimation of 2.
-Single-channel mode: use only HBFILTER_A
-Dual-channel mode: use both HBFILTER_A and HBFILTER_B

3: This requires the LFSR to be enabled: <EN_LFSR>=1.

4: EN_AMPDITH = 1 and EN_PHSDITH = 1 are recommended for the best performance.

5: DER is the decimation filters defined by the FIR A or FIR B filter. If the up-converter is not enabled (disabled), output is I/Q data.

6: DDC and NCO are enabled. For DDC function, bits 0, 2 and 5 need to be enabled all together.

REGISTER 5-42: ADDRESS 0X81 – DIGITAL DOWN-CONVERTER CONTROL 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FDR_BAND	EN_DDC2	GAIN_HBF_DDC	SEL_FDR	SEL_DSPP	8CH_CW	GAIN_8CH<1:0>	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **FDR_BAND:** Select 1st or 2nd Nyquist band

`1` = 2nd Nyquist band
`0` = 1st Nyquist band **(Default)**

bit 6 **EN_DDC2:** Enable DDC2 after the digital half-band filter (HBF) in DDC (MCP37D11-200).

`1` = Enabled
`0` = Disabled **(Default)**

bit 5 **GAIN_HBF_DDC:** Gain select for the output of the digital half-band filter (HBF) in DDC (MCP37D11-200) **(Note 1)**

`1` = x2
`0` = x1 **(Default)**

bit 4 **SEL_FDR:** Select fractional delay recovery (FDR) for eight-channel or dual-channel mode **(Note 2, Note 3)**

`1` = FDR for eight-channel
`0` = FDR for dual-channel **(Default)**

bit 3 **SEL_DSPP:** Select digital signal post-processing (DSPP) features for eight-channel or dual-channel mode **(Note 2, Note 3)**

`1` = DSPP for eight-channel
`0` = DSPP for dual-channel **(Default)**

bit 2 **8CH_CW:** Enable CW mode in octal-channel mode (MCP37D11-200) **(Note 3, Note 4)**

`1` = Enabled
`0` = Disabled **(Default)**

bit 1-0 **GAIN_8CH<1:0>:** Select gain factor for CW signal in octal-channel modes.

`11` = x8, `10` = x4, `01` = x2, `00` = x1 **(Default)**

Note 1: The half-band filters (HBF) are used by splitting a full-band signal of bandwidth B into two half-bandwidth (B/2). Since the bandwidth is reduced by a factor of 2, the sampling rate requirement is also reduced by a factor of 2, which is equivalent to oversampling by a factor of 2 (x2). The HBFs are used in the sub-band coding of digital video and audio signal applications. Also used for digital interpolation and decimation in signal processing.

2: Fractional delay compensates digitally for the sampling skew caused by round-robin style sampling of the inputs. See **Section 4.8.1 “Fractional Delay Recovery for Dual and Octal-Channel Modes”** for details.

3: By enabling this bit, the phase offset corrections in Address 0x086 – 0x095 (Registers 5-47 – 5-62) are also enabled. SEL_DSPP is a global set bit to enable SEL_FDR bit and LVDS_8CH bit (Address 0x62 – Register 5-20).

4: When CW mode is enabled, the ADC output is the result of the summation (addition) of all eight channel data after each channel’s digital phase offset, digital gain and digital offset are controlled using the Address 0x86 - 0xA7 (Registers 5-47 to 5-79). The result is similar to the beamforming in the phased-array sensors.

REGISTER 5-43: ADDRESS 0X82 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE <7:0>:** Lower byte of NCO_TUNE<31:0> **(Note 2).**
`0000-0000` = DC (0 Hz) when NCO_TUNE<31:0> = `0000 0000` **(Default)**

Note 1: This register is used only when DDC is enabled: EN_DDC1 = `1` in Address 0x80 (Register 5-41). See **Section 4.8.4.4 “Numerically Controlled Oscillator (NCO)”** for the details of NCO. This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: NCO frequency = (NCO_TUNE<31:0>/2^{32}) x f_S/2, where f_S is the sampling clock frequency.

REGISTER 5-44: ADDRESS 0X83 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<15:8>:** Middle lower byte of NCO_TUNE<31:0> **(Note 2).**
`0000-0000` = **Default**

Note 1: This register is used only when DDC is enabled: EN_DDC1 = `1` in Address 0x80 (Register 5-41). See **Section 4.8.4.4 “Numerically Controlled Oscillator (NCO)”** for the details of NCO. This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: NCO frequency = (NCO_TUNE<31:0>/2^{32}) x f_S/2, where f_S is the sampling clock frequency.

REGISTER 5-45: ADDRESS 0X84 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (MIDDLE UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<23:16>:** Middle upper byte of NCO_TUNE<31:0> (**Note 2**)
`0000-0000` = **Default**

Note 1: This register is used only when DDC is enabled: EN_DDC1 = `1` in Address 0x80 (Register 5-41). See **Section 4.8.4.4 “Numerically Controlled Oscillator (NCO)”** for the details of NCO. This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: NCO frequency = (NCO_TUNE<31:0>/2^{32}) x $f_S/2$, where f_S is the sampling clock frequency.

REGISTER 5-46: ADDRESS 0X85 – NUMERICALLY CONTROLLED OSCILLATOR (NCO) TUNING (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NCO_TUNE<31:24>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **NCO_TUNE<31:24>:** Upper byte of NCO_TUNE<31:0> (**Note 2**).
`1111-1111` = $f_S/2$ if NCO_TUNE<31:0> = 0xFFFF FFFF
•
•
•
`0000-0000` = **Default**

Note 1: This register is used only when DDC is enabled: EN_DDC1 = `1` in Address 0x80 (Register 5-41). See **Section 4.8.4.4 “Numerically Controlled Oscillator (NCO)”** for the details of NCO.This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: NCO frequency = (NCO_TUNE<31:0>/2^{32}) x $f_S/2$, where f_S is the sampling clock frequency.

REGISTER 5-47: ADDRESS 0X86 – CH0 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1, Note 2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH0_NCO_PHASE<7:0>:** Lower byte of CH0_NCO_PHASE<15:0> **(Note 3)**

`1111-1111` = 1.4° when CH0_NCO_PHASE<15:0> = 0x00FF

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`0000-0000` = 0° when CH0_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: This register (Addresses 0x86 – 0xA7, Registers 5-47 – 5-79) has effect only when the following modes are used:

- CW with DDC mode in octal-channel mode
- Single and dual-channel mode with DDC

See 8CH_CW bit setting in Address 0x81 (Register 5-42). See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings. This register has effect for the MCP37D11-200 only and no effect for the MCP37211-200.

2: CH0 is the 1st channel selected by CH_ORDER<23:0>.

3: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-48: ADDRESS 0X87: CH0 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH0_NCO_PHASE<15:8>:** Upper byte of CH0_NCO_PHASE<15:0> **(Note 2)**

`1111-1111` = 359.995° when CH0_NCO_PHASE<15:0> = 0xFFFF

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`0000-0000` = 0° when CH0_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Notes 1 and 2 in Register 5-47.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-49: ADDRESS 0X88 – CH1 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH1_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH1_NCO_PHASE<7:0>:** Lower byte of CH1_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH1_NCO_PHASE<15:0> = 0x00FF

•
•
•

`0000-0000` = 0° when CH1_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH1 is the 2nd channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-50: ADDRESS 0X89 – CH1 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH1_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH1_NCO_PHASE <15:8>:** Upper byte of CH1_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH1_NCO_PHASE<15:0> = 0xFFFF

•
•
•

`0000-0000` = 0° when CH1_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH1 is the 2nd channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-51: ADDRESS 0X8A – CH2 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH2_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH2_NCO_PHASE<7:0>:** Lower byte of CH2_NCO_PHASE<15:0> **(Note 2)**

`1111-1111` = 1.4° when CH2_NCO_PHASE<15:0> = 0x00FF

-
-
-

`0000-0000` = 0° when CH2_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH2 is the 3rd channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-52: ADDRESS 0X8B – CH2 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH2_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH2_NCO_PHASE <15:8>:** Upper byte of CH2_NCO_PHASE<15:0> **(Note 2)**

`1111-1111` = 359.995° when CH2_NCO_PHASE<15:0> = 0xFFFF

-
-
-

`0000-0000` = 0° when CH2_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Registers 5-47. CH2 is the 3rd channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-53: ADDRESS 0X8C – CH3 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH3_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH3_NCO_PHASE<7:0>:** Lower byte of CH3_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH3_NCO_PHASE<15:0> = 0x00FF
•
•
•
`0000-0000` = 0° when CH3_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See **Note 1** in Register 5-47. CH3 is the 4th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-54: ADDRESS 0X8D – CH3 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH3_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH3_NCO_PHASE <15:8>:** Upper byte of CH3_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH3_NCO_PHASE<15:0> = 0xFFFF
•
•
•
`0000-0000` = 0° when CH3_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH3 is the 4th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-55: ADDRESS 0X8E – CH4 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH4_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH4_NCO_PHASE<7:0>:** Lower byte of CH4_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH4_NCO_PHASE<15:0> = 0x00FF

•

•

•

`0000-0000` = 0° when CH4_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH4 is the 5th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-56: ADDRESS 0X8F – CH4 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH4_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH4_NCO_PHASE <15:8>:** Upper byte of CH4_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH4_NCO_PHASE<15:0> = 0xFFFF

•

•

•

`0000-0000` = 0° when CH4_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH4 is the 5th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-57: ADDRESS 0X90 – CH5 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH5_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH5_NCO_PHASE<7:0>:** Lower byte of CH5_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH5_NCO_PHASE<15:0> = 0x00FF

•
•
•

`0000-0000` = 0° when CH5_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH5 is the 6th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-58: ADDRESS 0X91 – CH5 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH5_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH5_NCO_PHASE <15:8>:** Upper byte of CH5_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH5_NCO_PHASE<15:0> = 0xFFFF

•
•
•

`0000-0000` = 0° when CH5_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH5 is the 6th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-59: ADDRESS 0X92 – CH6 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH6_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH6_NCO_PHASE<7:0>:** Lower byte of CH6_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH6_NCO_PHASE<15:0> = 0x00FF

•

•

•

`0000-0000` = 0° when CH6_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH6 is the 7th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-60: ADDRESS 0X93 – CH6 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH6_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH6_NCO_PHASE <15:8>:** Upper byte of CH6_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH6_NCO_PHASE<15:0> = 0xFFFF

•

•

•

`0000-0000` = 0° when CH6_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH6 is the 7th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-61: ADDRESS 0X94 – CH7 NCO PHASE OFFSET IN CW OR DDC MODE (LOWER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH7_NCO_PHASE<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH7_NCO_PHASE<7:0>:** Lower byte of CH7_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 1.4° when CH7_NCO_PHASE<15:0> = 0x00FF

-
-
-

`0000-0000` = 0° when CH7_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH7 is the 8th channel selected by CH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-62: ADDRESS 0X95 – CH7 NCO PHASE OFFSET IN CW OR DDC MODE (UPPER BYTE) (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH7_NCO_PHASE<15:8>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH7_NCO_PHASE <15:8>:** Upper byte of CH7_NCO_PHASE<15:0> (**Note 2**)

`1111-1111` = 359.995° when CH7_NCO_PHASE<15:0> = 0xFFFF

-
-
-

`0000-0000` = 0° when CH7_NCO_PHASE<15:0> = 0x0000 **(Default)**

Note 1: See Note 1 in Register 5-47. CH7 is the 8th channel selected byCH_ORDER<23:0> bits.

2: CH(n)_NCO_PHASE_OFFSET<15:0> = 2^{16} x Phase Offset Value/360.

REGISTER 5-63: ADDRESS 0X96 – CH0 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH0_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH0_DIG_GAIN<7:0>:** Digital gain setting for channel 0 **(Note 2, Note 3)**

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH0 is the 1st channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: This register’s bits can be preprogrammed at the factory.

3: Max = 0x7F(3.96875), Min = 0x80 (-4), Step size = 0x01 (0.03125). Bits from 0x81-0xFF are two’s complementary of 0x00-0x80. Negative gain setting inverts output.

REGISTER 5-64: ADDRESS 0X97 – CH1 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH1_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH1_DIG_GAIN<7:0>:** Digital gain setting for channel 1 (**Note 2**)
`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH1 is the 2nd channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-65: ADDRESS 0X98 – CH2 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH2_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH2_DIG_GAIN<7:0>:** Digital gain setting for channel 2 (**Note 2**)

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH2 is the 3rd channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-66: ADDRESS 0X99 – CH3 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH3_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH3_DIG_GAIN<7:0>:** Digital gain setting for channel 3 (**Note 2**)

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH3 is the 4th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-67: ADDRESS 0X9A – CH4 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH4_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH4_DIG_GAIN<7:0>:** Digital gain setting for channel 4 **(Note 2)**

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH4 is the 5th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-68: ADDRESS 0X9B – CH5 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH5_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH5_DIG_GAIN<7:0>:** Digital gain setting for channel 5 (**Note 2**)

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH5 is the 6th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-69: ADDRESS 0X9C – CH6 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH6_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH6_DIG_GAIN<7:0>:** Digital gain setting for channel 6 **(Note 2)**

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH6 is the 7th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-70: ADDRESS 0X9D – CH7 DIGITAL GAIN (Note 1)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
CH7_DIG_GAIN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH7_DIG_GAIN<7:0>:** Digital gain setting for channel 7 (**Note 2**)

`1111-1111` = -0.03125
`1111-1110` = -0.0625
`1111-1101` = -0.09375
`1111-1100` = -0.125
•
•
•
`1000-0011` = -3.90625
`1000-0010` = -3.9375
`1000-0001` = -3.96875
`1000-0000` = -4
`0111-1111` = 3.96875 (MAX)
`0111-1110` = 3.9375
`0111-1101` = 3.90625
`0111-1100` = 3.875
•
•
•
`0011-1100` = 1.875 **(Default)**
•
•
•
`0000-0011` = 0.09375
`0000-0010` = 0.0625
`0000-0001` = 0.03125
`0000-0000` = 0.0

Note 1: CH7 is the 8th channel selected by CH_ORDER<23:0> bits. See Addresses 0x7D - 0x7F (Registers 5-38 – 5-40) for channel selection bit settings.

2: See Notes 2 and 3 in Register 5-63.

REGISTER 5-71: ADDRESS 0X9E – CH0 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH0_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 0 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.

2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-72: ADDRESS 0X9F – CH1 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH1_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH1_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 1 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.

2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-73: ADDRESS 0XA0 – CH2 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH2_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH2_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 2 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 or the corresponding channel.
2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-74: ADDRESS 0XA1 – CH3 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH3_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH3_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 3 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.
2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-75: ADDRESS 0XA2 – CH4 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH4_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH4_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 4 (**Note 2**)

`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>

•

•

•

`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>

`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.

2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-76: ADDRESS 0XA3 – CH5 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH5_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH5_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 5 (**Note 2**)

`1111-1111` = 0x01 x DIG_OFFSET_WEIGHT<1:0>

•

•

•

`0000-0001` = 0xFF x DIG_OFFSET_WEIGHT<1:0>

`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.

2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-77: ADDRESS 0XA4 – CH6 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH6_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH6_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 6 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0**(Default)**

Note 1: See Table 4-16 for the corresponding channel.
2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-78: ADDRESS 0XA5 – CH7 DIGITAL OFFSET (Note 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH7_DIG_OFFSET<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CH7_DIG_OFFSET <7:0>:** Digital offset setting bits for channel 7 (**Note 2**)
`1111-1111` = 0xFF x DIG_OFFSET_WEIGHT<1:0>
•
•
•
`0000-0001` = 0x01 x DIG_OFFSET_WEIGHT<1:0>
`0000-0000` = 0 **(Default)**

Note 1: See Table 4-16 for the corresponding channel.
2: Offset value is two’s complement. This value is multiplied by DIG_OFFSET_WEIGHT<1:0> in Address 0xA7 (Register 5-79).

REGISTER 5-79: ADDRESS 0XA7 – DIGITAL OFFSET WEIGHT CONTROL

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
FCB<5:3>			DIG_OFFSET_WEIGHT<1:0>		FCB<2:0>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-5 **FCB<7:5>:** Factory-controlled bits. This is not for the user. Do not program.

bit 4-3 **DIG_OFFSET_WEIGHT<1:0>**: Control the weight of the digital offset settings **(Note 1)**
`11` = 2 LSB x Digital Gain
`10` = LSB x Digital Gain
`01` = LSB/2 x Digital Gain
`00` = LSB/4 x Digital Gain, **(Default)**

bit 2-0 **FCB<2:0>:** Factory-controlled bits. This is not for the user. Do not program.

Note 1: This bit setting is used for the digital offset setting registers in Addresses 0x9E - 0xA5 (Registers 5-71 – 5-78).

REGISTER 5-80: ADDRESS 0XC0 – CALIBRATION STATUS INDICATION

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
CAL_STAT	FCB<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **CAL_STAT:** Power-up auto-calibration status indication flag bit
`1` = Device power-up calibration is completed
`0` = Device power-up calibration is not completed

bit 6-0 **FCB<6:0>:** Factory-controlled bits. These bits are readable, but have no meaning for the user.

REGISTER 5-81: ADDRESS 0XD1 – PLL CALIBRATION AND STATUS INDICATION

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
FCB<4:3>		PLL_CAL_STAT	FCB<2:1>		PLL_VCOL_STAT	PLL_VCOH_STAT	FCB<0>
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **FCB<4:3>:** Factory-controlled bits. These bits are readable, but have no meaning for the user.

bit 5 **PLL_CAL_STAT:** PLL auto-calibration status indication flag bit **(Note 1)**
`1` = Complete: PLL auto-calibration is completed
`0` = Incomplete: PLL auto-calibration is not completed

bit 4-3 **FCB<2:1>:** Factory-controlled bits. These bits are readable, but have no meaning for the user.

REGISTER 5-81: ADDRESS 0XD1 – PLL CALIBRATION AND STATUS INDICATION (CONTINUED)

bit 2 **PLL_VCOL_STAT:** PLL drift status indication bit
`1` = PLL drifts out of lock with low VCO frequency
`0` = PLL operates as normal

bit 1 **PLL_VCOH_STAT:** PLL drift status indication bit
`1` = PLL drifts out of lock with high VCO frequency
`0` = PLL operates as normal

bit 0 **FCB<0>:** Factory-controlled bits. This bit is readable, but have no meaning for the user.

Note 1: See PLL_CALTRIG bit setting in Address 0x6B (Register 5-27).

REGISTER 5-82: ADDRESS 0X15C – CHIP ID (LOWER BYTE) (Note 1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CHIP_ID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CHIP_ID<7:0>:** Chip ID of the device: Lower byte of the CHIP ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.

Example: MCP37231-200: ‘0000 1000 0111 0000’
MCP37221-200: ‘0000 1000 0101 0000’
MCP37211-200: ‘0000 1000 0011 0000’
MCP37D31-200: ‘0000 1010 0111 0000’
MCP37D21-200: ‘0000 1010 0101 0000’
MCP37D11-200: ‘0000 1010 0011 0000’

REGISTER 5-83: ADDRESS 0X15D – CHIP ID (UPPER BYTE) (Note 1)

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x
CHIP_ID<15:8>							
bit 7							bit 0

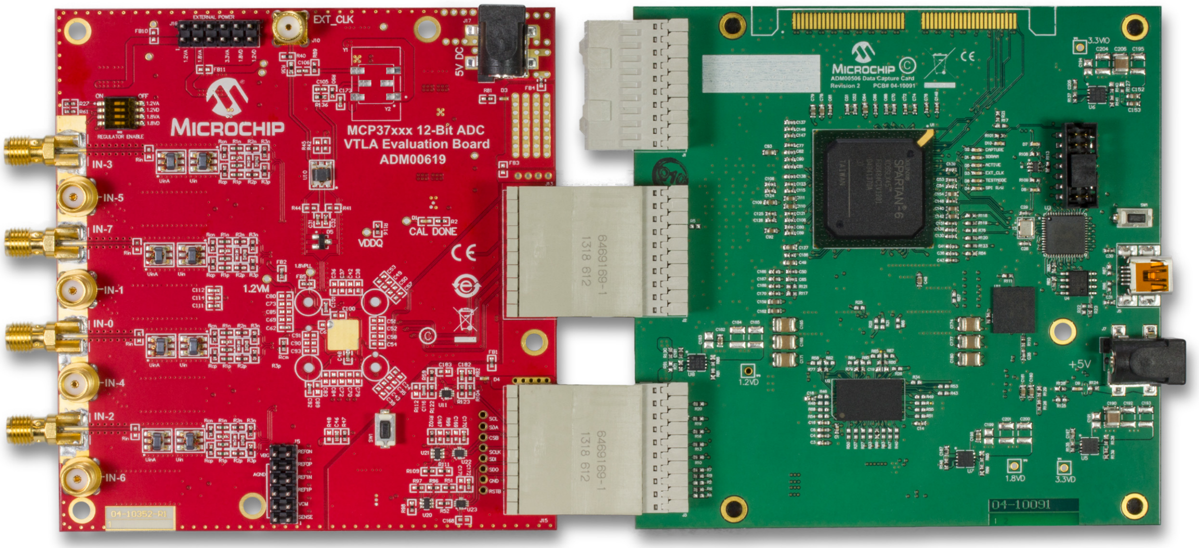
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-0 **CHIP_ID<15:8>:** Chip ID of the device: Upper byte of the CHIP ID<15:0>

Note 1: Read-only register. Preprogrammed at the factory for internal use.
See example in Note 1 in Register 5-82.

6.0 DEVELOPMENT SUPPORT

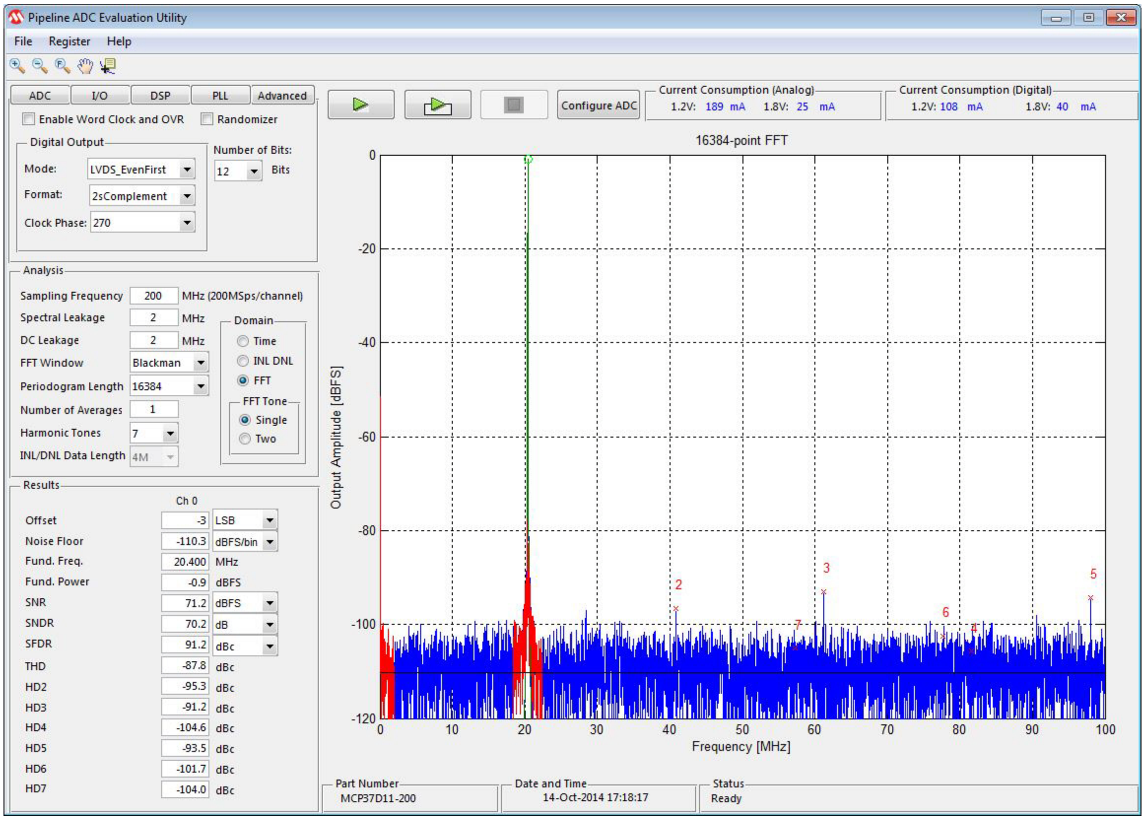
Microchip offers a high-speed ADC evaluation platform which can be used to evaluate Microchip's high-speed ADC products. The platform consists of an MCP37XXX evaluation board, an FPGA-based data capture card board and a PC-based Graphical User Interface (GUI) software for ADC configuration and evaluation. Figures 6-1 and 6-2 show this evaluation tool. This evaluation platform allows users to quickly evaluate the ADC's performance for their specific application requirements. More information is available at http://www.microchip.com.



(a) MCP37X1X-200, 12-Bit 200 Msps ADC VTLA Evaluation Board

(b) MCP37XXX High-Speed Pipeline ADC Data Capture Card

FIGURE 6-1: *12-Bit ADC Evaluation Board shown with High-Speed Data Capture Card.*



☐ Enable Word Clock and OVR ☐ Randomizer

Digital Output

Mode: LVDS_EvenFirst

Format: 2sComplement

Clock Phase: 270

Number of Bits: 12 Bits

Current Consumption (Analog) 1.2V: 189 mA 1.8V: 25 mA

Current Consumption (Digital) 1.2V: 108 mA 1.8V: 40 mA

Analysis

Sampling Frequency 200 MHz (200MSps/channel)

Spectral Leakage 2 MHz

DC Leakage 2 MHz

FFT Window Blackman

Periodogram Length 16384

Number of Averages 1

Harmonic Tones 7

INL/DNL Data Length 4M

Domain: ○ Time ○ INL DNL ● FFT

FFT Tone: ● Single ○ Two

Results

	Ch 0	
Offset	-3	LSB
Noise Floor	-110.3	dBFS/bin
Fund. Freq.	20.400	MHz
Fund. Power	-0.9	dBFS
SNR	71.2	dBFS
SNDR	70.2	dB
SFDR	91.2	dBc
THD	-87.8	dBc
HD2	-95.3	dBc
HD3	-91.2	dBc
HD4	-104.6	dBc
HD5	-93.5	dBc
HD6	-101.7	dBc
HD7	-104.0	dBc

Part Number: MCP37D11-200

Date and Time: 14-Oct-2014 17:18:17

Status: Ready

FIGURE 6-2: *PC-Based Graphical User Interface Software.*

NOTES:

7.0 TERMINOLOGY

Analog Input Bandwidth (Full Power Bandwidth)

The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay or Sampling Delay

This is the time delay between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty

The sample-to-sample variation in aperture delay.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal-to-noise ratio due to the jitter alone will be:

EQUATION 7-1:

$$SNR_{JITTER} = -20log(2\pi \times f_{IN} \times t_{JITTER})$$

Calibration Algorithms

This device utilizes two patented analog and digital calibration algorithms, Harmonic Distortion Correction (HDC) and DAC Noise Cancellation (DNC), to improve the ADC performance. The algorithms compensate various sources of linear impairments such as capacitance mismatch, charge injection error and finite gain of operational amplifiers. These algorithms execute in both power-up sequence (foreground) and background mode:

- Power-Up Calibration: The calibration is conducted within the first 2^{27} clock cycles after power-up. The user needs to wait this Power-Up Calibration period, after the device is powered up, for an accurate ADC performance.
- Background Calibration: This calibration is conducted in background while the ADC is performing conversions. The update rate is about every 2^{30} clock cycles.

Channel Crosstalk

This is a measure of the internal coupling of a signal from an adjacent channel into the channel of interest in the multi-channel mode. It is measured by applying a full-scale input signal in the adjacent channel. Crossalk is the ratio of the power of the coupling signal (as measured at the output of the channel of interest) to the power of the signal applied at the adjacent channel input. It is typically expressed in dBc.

Pipeline Delay (LATENCY)

LATENCY is the number of clock cycles between the initiation of conversion and when that data is presented to the output driver stage. Data for any given sample is available after the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the Pipeline Delay plus the Output Delay.

Clock Pulse Width and Duty Cycle

The clock duty cycle is the ratio of the time the clock signal remains at a logic high (clock pulse width) to one clock period. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

Differential Nonlinearity (DNL, No Missing Codes)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. No missing codes to 12-bit resolution indicates that all 4096 codes must be present over all the operating conditions.

Integral Nonlinearity (INL)

INL is the maximum deviation of each individual code from an ideal straight line drawn from negative full scale through positive full scale.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), below the Nyquist frequency and excluding the power at DC and the first nine harmonics.

EQUATION 7-2:

$$SNR = 10log\left(\frac{P_S}{P_N}\right)$$

SNR is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D) below the Nyquist frequency, but excluding DC:

EQUATION 7-3:

$$SINAD = 10\log\left(\frac{P_S}{P_D + P_N}\right) = -10\log\left[10^{-\frac{SNR}{10}} - 10^{-\frac{THD}{10}}\right]$$

SINAD is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the converter full-scale range.

Effective Number of Bits (ENOB)

The effective number of bits for a sine wave input at a given input frequency can be calculated directly from its measured SINAD using the following formula:

EQUATION 7-4:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Gain Error

Gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

Gain error is usually expressed in LSB or as a percentage of full-scale range (%FSR).

Gain-Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature, typically expressed in ppm/°C.

Offset Error

The major carry transition should occur for an analog value of ½ LSB below $A_{IN}+ = A_{IN}-$. Offset error is defined as the deviation of the actual transition from that point.

Temperature Drift

The temperature drift for offset error and gain error specifies the maximum change from the initial (+25°C) value to the value at across the T_{MIN} to T_{MAX} range.

Maximum Conversion Rate

The maximum clock rate at which parametric testing is performed.

Minimum Conversion Rate

The minimum clock rate at which parametric testing is performed.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier) or dBFS.

Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental (P_S) to the summed power of the first 13 harmonics (P_D).

EQUATION 7-5:

$$THD = 10\log\left(\frac{P_S}{P_D}\right)$$

THD is typically given in units of dBc (dB to carrier). THD is also shown by:

EQUATION 7-6:

$$THD = -20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_1^2}$$

Where:

V_1 = RMS amplitude of the fundamental frequency

V_1 through V_n = Amplitudes of the second through nth harmonics

Two-Tone Intermodulation Distortion (Two-Tone IMD, IMD3)

Two-tone IMD is the ratio of the power of the fundamental (at frequencies f_{IN1} and f_{IN2}) to the power of the worst spectral component at either frequency $2f_{IN1} - f_{IN2}$ or $2f_{IN2} - f_{IN1}$. Two-tone IMD is a function of the input amplitudes and frequencies (f_{IN1} and f_{IN2}). It is either given in units of dBc (dB to carrier), when the absolute power of the fundamental is used as the reference, or dBFS (dB to full-scale), when the power of the fundamental is extrapolated to the ADC full-scale range.

Power Supply Rejection Ratio (PSRR)

Measured as the ratio of the change in the power supply voltage to the change in the ADC output.

- **AC PSRR:**

EQUATION 7-7:

$$PSRR_{AC} = 20log\left(\frac{\Delta AV_{DD}}{\Delta V_{OUT}}\right)$$

The AC PSRR is typically given in units of dBc.

- **DC PSRR:**

The DC PSRR is typically given in units of mV/V or dB.

EQUATION 7-8:

$$PSRR_{DC} = 20log\left(\frac{\Delta AV_{DD}}{\Delta V_{OFFSET}}\right)$$

Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both sides of a differential input pair. The common-mode signal can be an AC or DC signal or a combination of the two. CMRR is measured using the ratio of the differential signal gain to the common-mode signal gain and expressed in dB with the following equation:

EQUATION 7-9:

$$CMRR = 20log\left(\frac{A_{DIFF}}{A_{CM}}\right)$$

Where:

A_{DIFF} = ∆Output Code/∆Differential Voltage

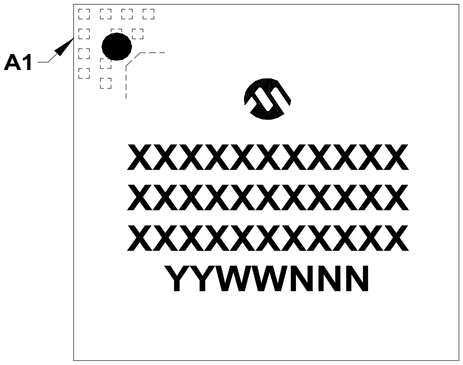
A_{DIFF} = ∆Output Code/∆Common Mode Voltage

NOTES:

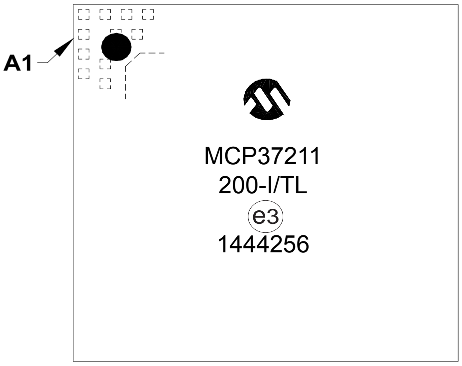
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

124-Lead VTLA (9 x 9 x 0.9 mm)



Example

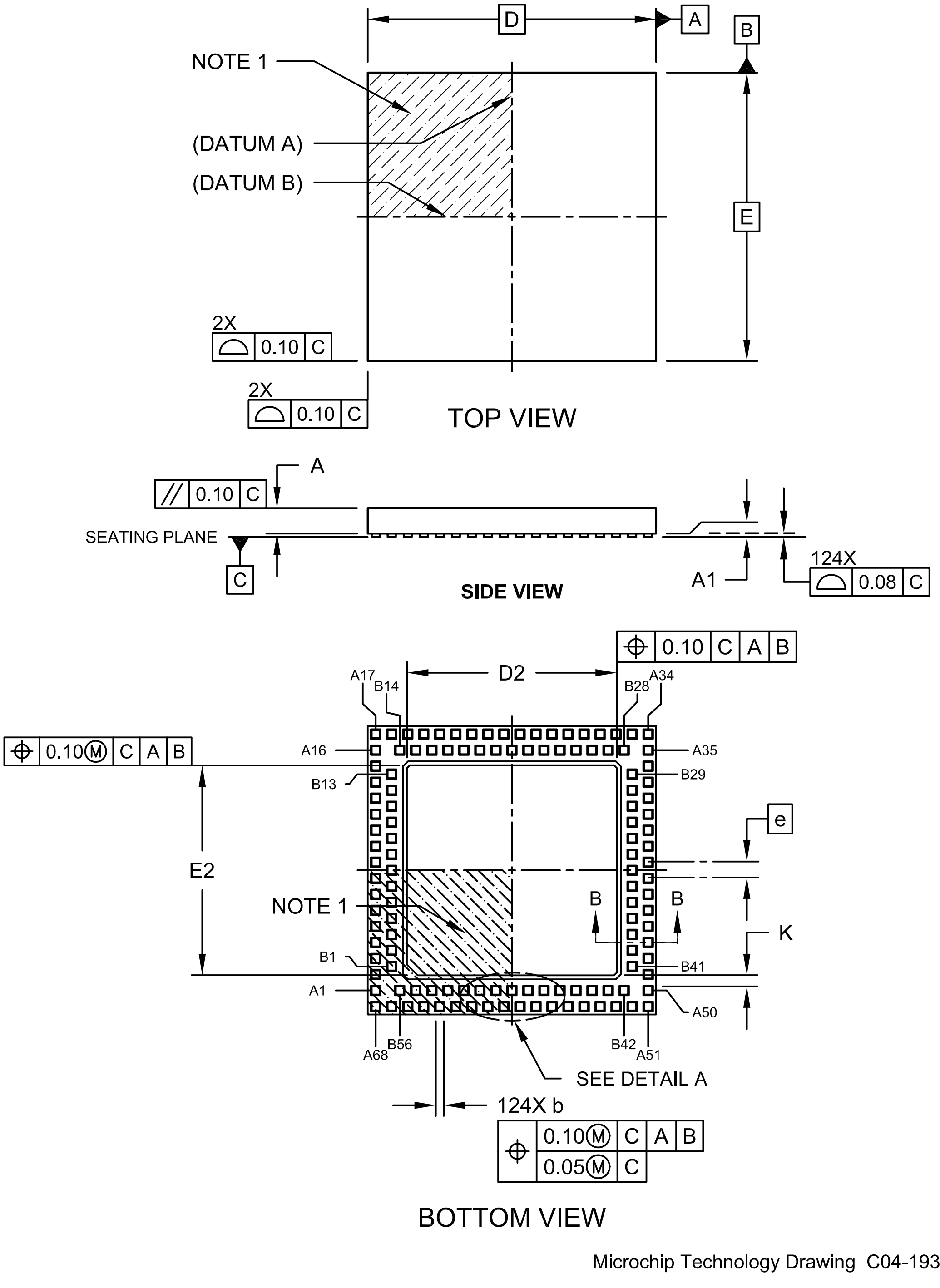


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

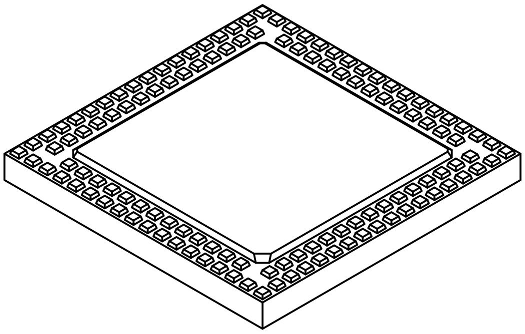
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

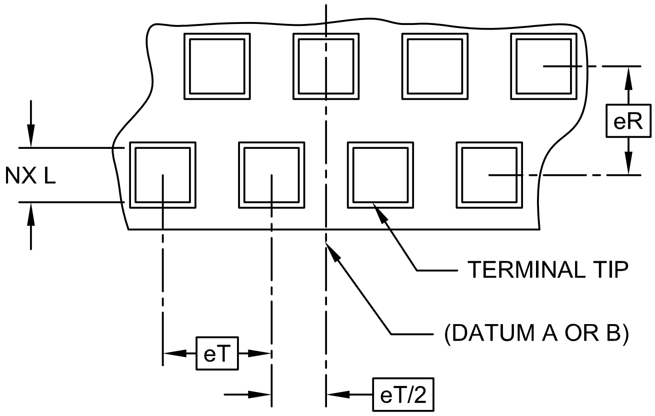


Microchip Technology Drawing C04-193A Sheet 1 of 2

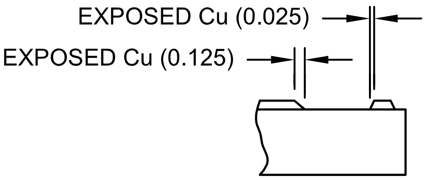
124-Terminal Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





DETAIL A



SECTION B-B

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N		124	
Pitch	eT		0.50 BSC	
Pitch (Inner to outer terminal ring)	eR		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	-	0.05
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	6.40	6.55	6.70
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	6.40	6.55	6.70
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.20	0.25	0.30
Contact-to-Exposed Pad	K	0.20	-	-

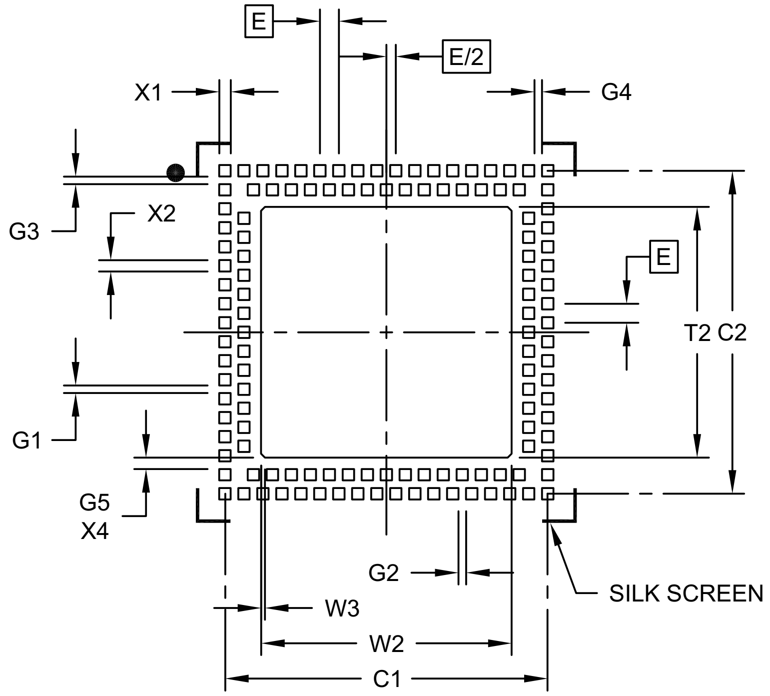
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-193A Sheet 2 of 2

124-Very Thin Leadless Array Package (TL) – 9x9x0.9 mm Body [VTLA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Pad Clearance	G1	0.20		
Pad Clearance	G2	0.20		
Pad Clearance	G3	0.20		
Pad Clearance	G4	0.20		
Contact to Center Pad Clearance (X4)	G5	0.30		
Optional Center Pad Width	T2			6.60
Optional Center Pad Length	W2			6.60
Optional Center Pad Chamfer (X4)	W3		0.10	
Contact Pad Spacing	C1		8.50	
Contact Pad Spacing	C2		8.50	
Contact Pad Width (X124)	X1			0.30
Contact Pad Length (X124)	X2			0.30

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2193A

APPENDIX A: REVISION HISTORY

Revision A (October 2014)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**-XXX**	**X**	**/XX**
Device	**Sample Rate**	**Temperature Range**	**Package**

Device: MCP37211-200: 12-Bit Low-Power ADC with 8-Channel MUX
MCP37D11-200: 12-Bit Low-Power ADC with 8-Channel MUX, Digital Down-Converter and CW Beamforming

Sample Rate: 200 = 200 Msps

Temperature Range: I = -40°C to +85°C (Industrial)

Package: TL = Terminal Very Thin Leadless Array Package - 9x9x0.9 mm Body (VTLA), 124-Lead
TE* = Ball Plastic Thin Profile Fine Pitch Ball Grid Array - 8x8x1.08 mm Body (TFBGA), 121-Lead

* Contact Microchip Technology Inc. for availability.

Examples:

a)	MCP37211-200I/TL:	200 Msps, Industrial Temperature, 124LD VTLA Package
b)	MCP37D11-200I/TE*:	200 Msps, Industrial Temperature, 121LD TFBGA Package
c)	MCP37D11-200I/TL:	200 Msps, Industrial temperature, 124LD VTLA Package

* Contact Microchip Technology Inc. for availability.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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